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(54) **A document acknowledge system having horizontal/vertical-run length smoothing algorithm circuits and a document region divide circuit**

Vorlagenerkennungssystem mit Schaltungen mit horizontalem/vertikalem Lauflängeglättungsalgorithmus und einer Schaltung zur Bereichsaufteilung von Vorlagen

Système de reconnaissance de documents ayant des circuits à algorithme de lissage de longueurs de série horizontales/verticales et un circuit pour la division d'un document en régions

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Description

BACKGROUND OF THE INVENTION

The present invention relates to a document acknowledge system, and more particularly, to a circuit for performing a horizontal run-length smoothing algorithm (H-RLSA) in a document acknowledge system, comprising memory means for storing digital data of a document and for outputting a stored data in a read mode, wherein the data outputted from the memory means are scanned horizontally in the memory means in order to get a horizontal run-length which represents horizontally adjacent black pixels.

It also relates to a circuit for performing a vertical run-length smoothing algorithm (V-RLSA) in a document acknowledge system, comprising memory means for storing digital data of a document and for outputting a stored data in a read mode and for changing a stored data in a write mode, wherein the data outputted from the memory means are scanned vertically in the memory means in order to get a vertical run-length which represents vertically adjacent black pixels.

It further relates to a circuit for performing a horizontal run-length smoothing algorithm (H-RLSA) and a vertical run-length smoothing algorithm (V-RLSA) in a document acknowledge system, and for combining the outputs of said H-RLSA and V-RLSA algorithm by ANDing the resulting outputs.

In these circuits, a horizontal run-length smoothing algorithm (H-RLSA) and/or a vertical run-length smoothing algorithm (V-RLSA) are performed by hardware, and the smoothed data is produced by hardware.

Conventionally, the document acknowledge system scans a document horizontally to store horizontal data, and then scans the document vertically to store vertical data. Then, the system performs a horizontal-run length smoothing algorithm process. By this process, while only binary data "1" succeeded above a predetermined number of times is maintained naturally, binary data "1" not succeeded above the predetermined number of times is canceled. For example, provided that the system scans the document, so that it stores the horizontal data "0001111000111111", and a threshold value is "5", the smoothed data "0000000000111111" is obtained, since only binary data "1" succeeded above 5 times is maintained naturally and binary data "1" not succeeded above 5 times is reset into binary data "0" by the horizontal-run length smoothing algorithm process.

Then, the document acknowledge system performs a vertical-run length smoothing algorithm process. Similarly, by this process, while only binary data "1" succeeded above a predetermined number of times is maintained naturally, binary data "1" not succeeded above the predetermined number of times is canceled. The smoothed data obtained from these processes then are divided by block unit. These divided results allow the document text and graphic region to be divided in accordance with height and width of the block.

However, in the above-mentioned coventional document acknowledge system, the horizontal-run length smoothing algorithm and vertical-run length smoothing algorithm are processed by software executed by a microprocessor and the smoothed data also is logical-produced by the software. Thus, the microprocessor in the system can be loaded with too much works, causing its efficiency to be reduced and its process to be run slowly.

Such a conventional document acknowledge system is described in the paper of S.N. SRIHARI, "Document image understanding", 1986 Proceedings "Fall joint computer conference", 2-6 NOV. 1986.

SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide a horizontal-run length smoothing algorithm circuit for smoothing horizontal data not with software executed by a microprocessor, but with hardware, the horizontal data stored by scanning a document horizontally.

Another object of the present Invention is to provide a vertical-run length smoothing algorithm circuit for smoothing vertical data not with software executed by a microprocessor, but with hardware, the vertical data stored by scanning the document vertically.

Still another object of the present invention is to provide a document region divide circuit for dividing a document region in which the smoothed data is logical-produced by hardware.

In accordance with the present invention, these objects can be accomplished by providing a circuit for performing a horizontal run-length smoothing algorithm (H-RLSA) in a document acknowledge system according to claim 1, a circuit for performing a vertical run-length smoothing algorithm (V-RLSA) in a document acknowledge system according to claim 6, or a circuit for performing a horizontal run-length smoothing algorithm (H-RLSA) and a vertical run-length smoothing algorithm (V-RLSA) in a document acknowledge system according to claim 12.

Further developments of the invention can be found in the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present Invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram of a horizontal-run length smoothing algorithm circuit of the present invention;
Fig. 2 Is a block diagram of a vertical-run length smoothing algorithm circuit of the present invention;
Fig. 3A and 3B illustrate tables of the original pixel data and the smoothed pixel data by the present

invention, respectively;

Fig. 4 illustrates a map of a V-RLSA memory shown in Fig. 2;

Fig. 5 is a flowchart of operation of the circuit shown in Fig. 2;

Fig. 6 is a block diagram of a document region divide circuit of the present invention;

Figs. 7A to 7F are waveform diagrams of respective outputs from components of the circuit shown in Fig. 6; and

Figs. 8A to 8C illustrate the pixel data of a H-RLSA memory and the V-RLSA memory of the circuit shown in Fig. 6 and the ANDed data of pixel data of the H-RLSA memory and the V-RLSA memory, respectively.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Fig. 1 is a block diagram of a horizontal-run length smoothing algorithm circuit of the present invention. As shown in the drawing, the horizontal-run length smoothing algorithm circuit comprises an address generating counter 110 for counting a system clock signal ϕ_1 to output the counted value as an address signal, a horizontal-run length smoothing algorithm (H-RLSA) memory 120 for storing horizontal data and inputting the address signal from the address generating counter 110, a count control unit 130 for applying the system clock signal ϕ_1 as a count clock signal and applying low voltage data to the H-RLSA memory 120, at write state of the H-RLSA memory 120 and for comparating read data with a reference signal B^+ to apply the system clock signal ϕ_1 as the count clock signal when the read data and the reference signal B^+ are the same and to output a comparison enable signal at initial state of the period that the read data and the reference signal B^+ are not the same, at read state of the H-RLSA memory 120, a read/write control unit 140 for counting up/down the system clock signal ϕ_1 outputted from the count control unit 130 in accordance with the read/write states of the H-RLSA memory 120 and comparating the counted value with a horizontal threshold value when the comparison enable signal is outputted from the count control unit 130 to output read/write control signals in response to the comparated results, and a write address setting unit 150 for substracting the counted value from the read/write control unit 140 from the output address value from the address generating counter 110 and then loading the subtracted value into the address generating counter 110, at initial state of period that the write control signal is outputted from the read/write control unit 140.

The count control unit 130 comprises a buffer 131 for applying low voltage data to the H-RLSA memory 120 at write state of the H-RLSA memory 120, a comparator 132 for comparating the read data with the reference signal B^+ at read state of the H-RLSA memory 120, an inverter 133 for inverting an output signal from one output terminal (A=B) of the comparator 132, an OR gate 134 for ORing an output signal from the inverter 133 and the system clock signal ϕ_1, an OR gate 135 for ORing the read/write control signals from the read/write control unit 140 to the H-RLSA memory 120 and the system clock signal ϕ_1, an AND gate 136 for ANDing output signals from the OR gates 134 and 135 to apply the ANDed signal as the count clock signal, and a mono-multivibrator 137 responsive to a output signal from the other terminal (A<B) of the comparator 132 for outputting the comparison enable pulse signal.

Also, the read/write control unit 140 comprises an up/down counter 141 for counting up/down the system clock signal ϕ_1 outputted from the count control unit 130 in accordance with the read/write states of the H-RLSA memory 120, a threshold setting unit 142 for setting the horizontal threshold value, a comparator 143 for comparating the counted value from the up/down counter 141 with the horizontal threshold value from the threshold setting unit 142 when the comparison enable signal is outputted from the count control unit 130, an inverter 144 for inverting a carry signal from the up/down counter 141, a flip-flop 145 responsive to an output signal from the inverter 144 for outputting the read control signal and responsive to an output signal from one output terminal (A<B) of the comparator 143 for outputting the write control signal, and mono-multivibrator 146 responsive to an output signal from the other terminal (A≥B) of the comparator 143 for generating a pulse signal to apply the pulse signal as a clear signal to the up/down counter 141.

Also, the write address setting unit 150 comprises a latch 151 responsive to the write control signal from the read/write control unit 140 for latching the address signal from the address generating counter 110, a subtracter 152 responsive to the write control signal from the read/write control unit 140 for subtracting the counted value from the read/write control unit 140 from an output signal from the latch 151 to apply the subtracted value as load data to the address generating counter 110, and a mono-multivibrator 153 responsive to the write control signal from the read/write control unit 140 for generating a pulse signal to apply the pulse signal as a load control signal to the address generating count 110.

Fig. 2 is a block diagram of a vertical-run length smoothing algorithm circuit of the present invention. As shown in the drawing, the vertical-run length smoothing algorithm circuit comprises a start address setting unit 210 for storing number of horizontal pixels as an offset value and number of vertical pixels, generating a carry signal as many as the number of vertical pixels whenever the read operation is completed, loading with and outputting a start address value, and incrementing the start address value whenever the carry signal is generated to output the next vertical column of the start address value, a system clock supplying unit 220 for supplying a system clock signal ϕ_1 until the carry signal is

generated as much as the offset value after the start address value is outputted from the start address setting unit 210, an address generating counter 230 responsive to the system clock signal ϕ_1 for loading with the start address value from the start address setting unit 210 and outputting an address signal, a vertical-run length smoothing algorithm (V-RLSA) memory 240 for storing vertical data and inputting the address signal from the address generating counter 230, resulting in being accessed, a count control unit 250 for applying the system clock signal ϕ_1 as a count clock signal and applying low voltage data of the V-RLSA memory 240, at write state of the V-RLSA memory 240 and for comparating read data with a reference signal B^+ to apply the system clock signal ϕ_1 as the count clock signal when the read data and the reference signal B^+ are the same and to output a comparison enable signal at initial state of the period that the read data and the reference signal B^+ are not the same, at read state of the V-RLSA memory 240, a read/write control unit 260 for counting up/down the system clock signal ϕ_1 outputted from the count control unit 250 in accordance with the read/write states of the V/RLSA memory 240 and comparating the counted value with a horizontal threshold value when the comparison enable signal is outputted from the count control unit 250 to output read/write control signals in response to the comparated results, and an address resetting unit 270 for adding the offset value from the start address setting unit 210 to the address signal value from the address generating counter 230 counter 230 in response to the system clock signal ϕ_1, multiplying the offset value from the start address setting unit 210 by the counted value from the read/write control unit 260 and then subtracting the multiplied value from the address signal value from the address generating counter 230, and loading the remaining value into the address generating counter 230 at initial state of the period that the write control signal is outputted from the read/write control unit 260.

The start address setting unit 210 comprises a latch 211 responsive to a horizontal control signal IO_1 for latching the number of horizontal pixels as the offset value, a latch 213 responsive to a vertical control signal IO_3 for latching the number of vertical pixels, an AND gate 218 responsive to the read control signal from the read/write control unit 260 for allowing the system clock signal ϕ_1 to be passed therethrough, a down counter 215 for inputting an output signal from the latch 213 as a load signal and counting down an output signal from the AND gate 218 to generate the carry signal, a buffer 217 responsive to the read control signal from the read/write control unit 280 for allowing the carry signal from the down counter 215 to be passed therethrough, an AND gate 216 for ANDing output signal from the buffer 217 and the vertical control signal IO_3 to apply the ANDed signal as a load control signal to the down counter 215, an up counter 212 for loading with the start address value in response to a start control signal IO_2 and counting up the carry signal from the down counter 215, and a buffer 214 responsive to an output signal from the AND gate 216 for allowing an output signal from the up counter 212 to be passed therethrough.

Also, the system clock supplying unit 220 comprises a flip-flop 223 for inputting the vertical control signal IO_3 as a clock signal to output a high voltage signal, an AND gate 225 for ANDing the high voltage signal from the flip-flop 223 and a reference clock signal ϕ to output the ANDed signal as the system clock signal ϕ_1, an up counter 224 for counting up the carry signal from the start address setting unit 210, a comparator 221 for comparating the counted value from the up counter 224 with the offset value from the start address setting unit 210, and a mono-multivibrator 222 responsive to an output signal from the terminal (A=B) of the comparator 221 for generating a pulse signal to apply the pulse signal as a clear signal to the flip-flop 223.

Also, the count control unit 250 comprises a buffer 251 for applying low voltage data to the V-RLSA memory 240 at write state of the V-RLSA memory 240, a comparator 252 for comparating the read data with the reference signal B^+ at read state of the V-RLSA memory 240, an AND gate 253 for ANDing the output signal from the one output terminal (A=B) of the comparator 252 and the system clock signal ϕ_1, a selector 254 for selecting one of an output signal from the AND gate 253 and the system clock signal ϕ_1 in accordance with the read/write states of the V-RLSA memory 240 to apply the selected signal as the count clock signal, and a mono-multivibrator 255 responsive to an output signal from the other terminal (A<B) of the comparator 252 for generating a pulse signal to apply the pulse signal as the comparison enable signal.

The read/write control unit 260 comprises an up/down counter 261 for counting up/down the system clock signal ϕ_1 outputted from the count control unit 250 in accordance with the read/write states of the V-RLSA memory 240, a threshold setting unit 264 for setting the vertical threshold value, an AND gate 262 for ANDing the comparison enable signal from the count control unit 250 and the carry signal from the start address setting unit 210, a comparator 263 enabled by an output signal from the AND gate 262 for comparating the counted value from the up/down counter 261 with the vertical threshold value from the threshold setting unit 264, a mono-multivibrator 266 responsive to an output signal from one output terminal (A≥B) of the comparator 263 for outputting a pulse signal, AND gate 267 for ANDing the pulse signal from the mono-multivibrator 266 and the carry signal from the up/down counter 261 to apply the ANDed signal as a clear signal to the up/down counter 261, an AND gate 265 for ANDing the carry signal from the up/down counter 261 and a reset signal RST, and a flip-flop 268 responsive to an output signal from the AND gate 265 for outputting the read control signal and responsive to an output signal from the other output terminal (A<B) of the comparator 263 for outputting the write control signal.

Also, the address resetting unit 270 comprises an adder 271 for adding the offset value from the start address setting unit 210 to the address signal value from the address generating counter 230, a multiplier 272 for multiplying the offset value by the counted value from the read/write control unit 260, a subtracter 273 for subtracting an output signal value of the multiplier 272 from the address signal value of the address generating counter 230, a mono-multivibrator 274 responsive to the write control signal from the read/write control unit 260 for generating a pulse signal, an inverter 275 for inverting an output enable signal from the start address setting unit 210, an inverter 276 for inverting the pulse signal from the mono-multivibrator 274, an OR gate 277 for ORing output signals from the inverters 275 and 276 and the system clock signal ϕ_1, a buffer 278 responsive to an output signal from the OR gate 277 for allowing an output signal from the adder 271 to be passed therethrough to apply the output signal from the adder 271 as a load signal to the address generating counter 230, and a buffer 279 responsive to the pulse signal from the mono-multivibrator 274 for allowing an output signal from the subtracter 273 to be passed therethrough to apply the output signal from the subtracter 273 as a load signal to the address generating counter 230.

Figs. 3A and 3B illustrate tables of the original pixel data of the V-RLSA memory 240 and the smoothed pixel data by the present invention in the case that the vertical threshold value is 3, respectively.

Fig. 4 illustrates a map of a V-RLSA memory 240 shown in Fig. 2 and Fig. 5 is a flowchart of operation of the vertical-run length smoothing algorithm circuit shown in Fig. 2.

Fig. 6 is a block diagram of a document region divide circuit of the present invention. As shown in the drawing, the document region divide circuit comprises a horizontal-run length smoothing algorithm (H-RLSA) circuit 100, a vertical-run length smoothing algorithm (V-RLSA) circuit 200, a system clock and address supplying unit 310 for supplying a system clock signal ϕ_1 in response to an end signal ES of the V-RLSA circuit 200, counting the system clock signal ϕ_1 to output the counted value as horizontal/vertical address signals, and stopping supplying the system clock signal ϕ_1 when the system clock signal ϕ_1 was outputted therefrom a predetermined number of times, an address and read/write selecting unit 320 responsive to the end signal ES of the V-RLSA circuit 200 for selecting any one of the horizontal address signal of the H-RLSA circuit 100, the vertical address signal of the V-RLSA circuit 200 and the counted value from the system clock and address supplying unit 310 to output the selected signal as horizontal/vertical address signals, selecting one of horizontal read/write control signals R/W of the H-RLSA circuit 100 and the system clock signal ϕ_1 to output the selected signal as the horizontal read/write control signals, and selecting one of vertical read/write control signals R/W of the V-RLSA circuit 200 and the end signal ES of the V-RLSA circuit 200 to output the selected signal as the vertical read/write control signals, a horizontal-run length smoothing algorithm (H-RLSA) memory 120 accessed by the horizontal address signal from the address and read/write selecting unit 320 and responsive to the horizontal read/write control signals for operating at read/write states, a vertical-run length smoothing algorithm (V-RLSA) memory 240 accessed by the vertical address signal from the address and read/write selecting unit 320 and responsive to the vertical read/write control signals for operating at read/write states, an AND gate 330 for ANDing output data from the H-RLSA memory 120 and V-RLSA memory 240 by bit unit, and a buffer 340 for allowing an output signal from the AND gate 330 to be passed therethrough during a half cycle of the system clock signal ϕ_1 to apply the output signal from the AND gate 330 as write data to the H-RLSA memory 120.

The system clock and address supplying unit 310 comprises an OR gate 311 for ORing the end signal ES of the V-RLSA circuit 200 and a reference clock signal ϕ, a flip-flop 312 for inputting an output signal from the OR gate 311 as a clock signal to output the output signal from the OR gate 311 as the system clock signal ϕ_1, an up counter 313 for counting up the system clock signal ϕ_1, to output the counted value as the horizontal/vertical address signals, and a down counter for counting down the system clock signal ϕ_1, a predetermined number of times to generate a carry signal to apply the carry signal as a clear signal to the flip-flop 312.

Also, the address and read/write selecting unit 320 comprises an inverter 312 for inverting the end signal ES of the V-RLSA circuit 200, a selector 322 responsive to the end signal ES of the V-RLSA circuit 200 for selecting one of the horizontal address signal of the H-RLSA circuit 100 and counted value from the system clock and address supplying unit 310 to output the selected signal as the horizontal address signal, a selector 323 responsive to the end signal ES of the V-RLSA circuit 200 for selecting one of the vertical address signal of the V-RLSA circuit 200 and the counted value from the system clock and address supplying unit 310 to output the selected signal as vertical address signal, a selector 324 responsive to the end signal ES of the V-RLSA circuit 200 for selecting one of horizontal read/write control signals R/W of the H-RLSA circuit 100 and the system clock signal ϕ_1 to output the selected signal as the horizontal read/write control signals, and a selector responsive to the end signal ES of the V-RLSA circuit 200 for selecting one of vertical read/write control signals R/W of the V-RLSA circuit 200 and an output signal of the inverter 321 to output the selected signal as the vertical read/write control signals.

Figs. 7A to 7F are waveform diagrams of respective outputs from components of the document region divide circuit shown in Fig. 6; and

Figs. 8A to 8C illustrate the pixel data of the H-RLSA memory 120 and the V-RLSA memory 240 of the document region divide circuit shown in Fig. 6 and the ANDed

data of pixel data of the H-RLSA memory 120 and the V-RLSA memory 240, respectively.

Now, operations of the horizontal/vertical-run length smoothing algorithm circuit and the document region divide circuit in accordance with the present invention will be described more detailed.

In operation, at initial state of powering on, the up/down counter 141 indicated in FIG. 1 generates at the carry terminal (RC) a carry signal of high voltage which is in turn inverted by the inverter 144 into a low voltage signal, and then applied as a present signal to the flip-flop 145. Therefore, the flip-flop 145 outputs a read control signal of high voltage, thus the H-RLSA memory 120 enters a read state, simultaneously the buffer 131 enters a cut-off state. Also, the comparator 132 enters an enable state, simultaneously the latch 151 and the subtracter 152 enter disable states, so that the mono-multivibrator 153 can not output any pulse signal. In this case, the up/down counter 141 functions as an up counter.

Accordingly, the address generating counter 110 counts the system clock signal ϕ_1 in order to address the locations of the H-RLSA memory 120, sequentially. Also, the data stored in the addressed location of the H-RLSA memory 120 is read out, the read out data is in turn applied to the input terminal A of the comparator 132 in order to be compared with the reference signal B^+ applied to the other input terminal (B). At this time, if the data applied to the other input terminal (A) of the comparator 132 is the same high voltage data as that of the reference signal B^+, a low voltage signal is outputted from the output terminal (A<B) of the comparator 132, also a high voltage signal is outputted from the other output terminal (A=B) thereof. The high voltage signal outputted from the output terminal (A=B) is inverted by the inverter 133 into a low voltage signal which is in turn applied to an input terminal of the OR gate 134, so that the system clock signal ϕ_1 is applied to an input terminal of the AND gate 136 through the OR gate 134. At this time, a high voltage signal outputted from the flip-flop 145 is also applied to the other input terminal of the AND gate 136 through the OR gate 135, so that the system clock signal ϕ_1 is applied as a count clock signal to the up/down counter 141 through the AND gate 136. Accordingly, the up/down counter 141 counts up the system clock signal ϕ_1.

As above described, the address generating counter 110 counts the system clock signal ϕ_1 in order to sequentially address the locations of the H-RLSA memory 120, and then if the data stored in the addressed location of the H-RLSA memory 120 is the same high voltage data as that of the reference signal B^+, the up/down counter 141 counts up the system clock signal ϕ_1. It is therefore known that the up/down counter 141 counts up the times of the data of high voltage read out from the H-RLSA memory 120.

On the other hand, if the data stored in the addressed location of the H-RLSA memory 120 is a low voltage data different from the reference signal B^+, the output signals from the comparator 132 are inverted so that the low voltage signal is outputted from the other output terminal (A=B) and the high voltage signal is outputted from the output terminal (A<B). Also, at initial output state of the high voltage signal from the output terminal (A<B), a low voltage pulse signal is outputted from the mono-multivibrator 137 which is in turn applied to the comparator 143 as a comparison enable signal. Thereafter, the comparator 143 compares the counted value from the up/down counter 141 with the horizontal threshold value from the threshold setting unit 142, and then outputs the comparing result signal at its output terminal (A<B). For example, if the threshold value is "3", and the counted value from the up/down counter 141 exceeds "3", the comparator 143 outputs a low voltage signal at its output terminal (A<B), and a high voltage signal at its other output terminal (A≥B). In initial output state of the high voltage signal from the output terminal (A≥B), a low voltage pulse signal is outputted from the mono-multivibrator 146 in order to clear the up/down counter 141, so that the counted value of "O" can be obtained from the counter 141, also the carry signal is outputted.

If the data read out from the H-RLSA memory 120 is a low voltage data different from that of the reference signal B^+, the output signals of the comparator 132 maintains the previous state, so that the low voltage signal will be outputted from the other output terminal (A=B), and the high voltage signal will be outputted from the output terminal (A<B). Thereafter, the low voltage signal outputted from the other output terminal (A=B) is inverted by the inverter 133 into a high voltage signal which is in turn applied to the input terminal of the OR gate 134. Accordingly, the OR gate 134 outputs a high voltage signal at its output terminal, and the OR gate 135 also outputs a high voltage signal, so that the AND gate 136 continuously outputs a high voltage signal, resulting in maintaining the counted value from the up/down counter 141 at "O".

On the other hand, when the threshold value is "3", and the counted value from the up/down counter 141 is below "3", the comparator 143 enters an enable state. Accordingly, the comparator 143 outputs a high voltage signal at its output terminal (A<B), and a low voltage signal at its output terminal (A≥B), also the flip-flop 145, to which the high voltage signal outputted at the output terminal (A<B) is applied as a clock signal, outputs a low voltage signal of the write control signal. The H-RLSA memory 120 enters the write state by the low voltage write control signal, simultaneously the buffer 131 is turned on, so that a low voltage data is applied to the H-RLSA memory 120. At this time, the comparator 132 enters a disable state, resulting in maintaining its previous output state, and then the latch 151 enters an enable state, the subtracter 152 also enters an enable state. Accordingly, the address signal value outputted from the address generating counter 110 is latched by the latch

151, thereafter the latched value from the latch 151 and the counted value from the up/down counter 141 are subtracted by the subtracter 152. The subtracted value from the subtracter 152 is applied to the address generating counter 110 as a load signal, also in initial output state of the low voltage signal from the flip-flop 145, the low voltage pulse signal from the mono-multivibrator 153 is applied to the address generating counter 110 as a load control signal, thus the load signal from the subtracter 152 is loaded into the address generating counter 110, thereafter outputted from the address generating counter 110 in response to the system clock signal ϕ_1 in order to address the locations of the H-RLSA memory 120. The addressed location of the H-RLSA memory 120 is a first addressed location of high voltage, so that the data of low voltage from the buffer 131 is written into.

At this time, the up/down counter 141 enters a down-count state by the low voltage signal which is previously outputted from the flip-flop 145, and in turn applied to an input terminal of the OR gate 135. Also, the system clock signal ϕ_1 is applied as a count clock signal to the up/down counter 141 by way of the OR gate 135 and the AND gate 136. Therefore, the up/down counter 141 counts down the system clock signal ϕ_1 in order to decrement the counted value.

Thereafter, when the system clock signal ϕ_1 is again applied to the address generating counter 110 which counts the system clock signal ϕ_1, and then addresses the second location of the H-RLSA memory 120. Therefore, a low voltage data can be written into the addressed location of the H-RLSA memory 120, also the up/down counter 141 can count down.

Consequently, when the counted value from the up/down counter 141 is "O", the up/down counter 141 can output a high voltage carry signal which is in turn inverted, by the inverter 144, into a low voltage signal in order to present the flip-flop 145. Thereafter, the flip-flop 145 can output a high voltage read signal in order that the read operation can be again carried out.

Thus, the horizontal-run length smoothing algorithm process is carried out by sequentially reading out the data in the location of the H-RLSA memory 120 corresponding to the each of addresses incremented by "1" at a time, and the maintaining the data when the data is a low voltage data or a high voltage data of a times succeeded above a predetermined number of times of the threshold value from the threshold setting unit 142, and writing the data, after inverting the data into a low voltage data, into the H-RLSA memory 120 when the data is a high voltage data of a times succeeded below a predetermined number of times of the threshold value from the threshold setting unit 142.

On the other hand, at initial vertical-run length smoothing algorithm process, the reset pulse signal (RST) of low voltage is applied to the AND gate 265 shown in FIG. 2, therefore the AND gate 265 outputs a low voltage signal in order to present the flip-flop 268, the flip-flop 268 can thus output a high voltage read control signal. Consequently, by the high voltage read control signal, the V-RLSA memory 240 enters a read state, simultaneously the buffer 251 enters a cut off state, also the comparator 252 enters an enable state. At this time, the selector 254 selects and outputs an output signal, also the up/down counter 261 functions as an up counter.

Also, the number of pixels to be horizontally accessed by the horizontal control signal IO_1 are latched by the latch 211, and then outputted from the latch 211. Furthermore, the start address signal by the start control signal IO_2 is loaded into the up counter 212, and then outputted from the up counter 212. The number of pixels to be vertically accessed by the vertical control signal IO_3 of low voltage pulse are also latched by the latch 213, and then outputted from the latch 213.

When the vertical control signal IO_3 of low voltage pulse is applied to the AND gate 216, the AND gate 216 outputs a low voltage pulse signal which is in turn applied to the down counter 215 as a load control signal. Therefore, the number of vertically directed pixels outputted from the latch 213 are loaded into the down counter 215, also a low voltage pulse signal outputted from the AND gate 216 is applied to the buffer 214 as a output enable signal. Thus the start address signal outputted from the up counter 212 is applied to the address generating counter 230 by way of the buffer 214, simultaneously the low voltage pulse signal outputted from the AND gate 216 is applied to the buffer 278 by way of the OR gate 277 after being inverted into a high voltage signal by the inverter 275. Therefore, the buffer 278 enters an output disable state, and the buffer 279 also enters an output disable state because the mono-multivibrator 274 outputs a high voltage signal.

Also, the vertical control signal IO_3 of low voltage pulse is applied to the flip-flop 223 as a clock signal, so that the flip-flop 223 outputs a high voltage signal which is in turn applied to an input terminal of the AND gate 225. Simultaneously, the reference clock signal O is supplied as a system clock signal O_1 by way of the AND gate 225. Therefore, the start address signal outputted from the buffer 214 is loaded into the address generating counter 230 during low voltage period, and then outputted from the address generating counter 230 in order to address the location of the V-RLSA memory 240 corresponding to the start address.

If the start address loaded into the up counter 212 is set as "1", the location of the V-RLSA memory 240 corresponding to the start address "1" is addressed, therefore the data stored in the location corresponding to the start address "1" will be read out. Also, in this case, the other conditions are supposed to be set as the pixel data of the V-RLSA memory 240 is as indicated in FIG. 3A, and the map of theV-RLSA memory 240 is as indicated in FIG. 4, also the offset value of the number of horizontal pixels latched by the latch 211 is "8", furthermore the number of the vertical pixels latched by the latch 213 is "9".

Therefore, the data read out at the location corresponding to the start address "1" will be the same high voltage data as that of the reference signal B+, so that the comparator 252 outputs a high voltage signal at its output terminal (A=B), and a low voltage signal at the other output terminal (A<B). Also, the high voltage signal outputted from the terminal (A=B) is applied to the input terminal of the AND gate 253 in order that the system clock signal O_1 is applied to the input terminal of the selector 254 through the AND gate 253. At this time, the selector 254 selects the input terminal (A) for inputting the system clock signal ϕ_1 applied to the input terminal (A) is applied to the up/down counter 261 as a count clock signal. Therefore, the up/down counter 261 counts up the system clock signal ϕ_1, and then the counted value "1" can be obtained.

Also, the high voltage signal outputted from the flip-flop 268 is applied to an input terminal of the AND gate 218, so that the system clock signal ϕ_1 is applied to the down counter 215 through the AND gate 218 as a count clock signal, and the counted value by the down counter 215 is "8".

Also, the start address value "1" outputted from the address generating counter 230 is added, by the adder 271, to the offset value "8" of the latch 211 in order to be the added value "9", and in turn applied to the buffer 278 which thereafter enters an output enable state resulting from outputting the low voltage signal from the OR gate 277 during the low voltage period of the system clock signal ϕ_1. The output signal "9" from the adder 271 is loaded into the address generating counter 230 through the buffer 278, and the loaded signal then addresses the location of the V-RLSA memory 240 corresponding to the address "9" which is the second address of the first column of the V-RLSA memory 240. Therefore, the data stored in the address "9" is read out. At this time, if the data is high voltage data as indicated in FIG. 3A, the comparator 252 outputs a high voltage signal at its output terminal (A=B), and a low voltage signal at its other output terminal (A<B). Therefore, as above described, the counted value by the up/down counter 261 which counts up the system clock signal ϕ_1 will be "2". Also, the counted value by the down counter 215 which counts down the system clock signal ϕ_1 will be "7".

As above described, the address "9" outputted from the address generating counter 230 is address, by the adder 171, to the offset value "8" of the latch 271 in order to be the added value "17", in turn loaded into the address generating counter 230 through the buffer 278. Thereafter, the loaded signal addresses the location of the V-RLSA memory 240 corresponding to the address "17" which is the third address of the first column of the V-RLSA memory 240. Thus the data stored in the location of the V-RLSA memory 240 corresponding to the address "17" is read out. At this time if the data is a low voltage as indicated in FIG. 3A, the data is different from the reference signl B+. Therefore, the output signals from the comparator 252 are inverted, so that the low voltage signal is outputted at the output terminal (A=B), and the high voltage signal is outputted at the other output terminal (A<B). Thus, the system clock signal ϕ_1 can not pass through the AND gate 253, so that the counted value by the up/down counter 261 will be maintained at the value "2" because the system clock signal can not be applied to the up/down counter 261. Also, at initial output state of the high voltage signal from the other output terminal (A<B) of the comparator 252, the multivibrator 255 outputs a low voltage pulse signal, resulting in a low voltage pulse signal output from the AND gate 262. The low voltage pulse signal from the AND gate 262 is in turn applied to the comparator 263 as a comparison enable signal. Therefore, the comparator 263 enters an enable state, so that the counted value from the up/down counter 261 is compared with the vertical threshold value from the threshold setting unit 264. At this time, if the counted value from the up/down counter 261 exceeds the threshold value from the threshold setting unit 264, the comparator 263 will output a high voltage signal at its output terminal (A≥B), and a low voltage signal at its other output terminal (A<B). Also, if the counted value from the up/down counter 261 is below the threshold value from the threshold setting unit 264, the comparator 263 will output a high voltage signal at the other output terminal (A<B), and a low voltage signal at the output terminal (A≥B).

For example, if the threshold value from the threshold setting unit 264 is "3", and the counted value from the up/down counter 261 is "2", the comparator 263 will output a high voltage signal at the other output terminal (A<B), and a low voltage signal at the output terminal (A≥B). The high voltage signal outputted from the other output terminal (A<B) of the comparator 263 is applied to the flip-flop 268 as a clock signal, so that the flip-flop 268 outputs a write control signal of low voltage by which the system clock signal ϕ_1 can not pass through the AND gate 218. Therefore the system clock signal ϕ_1 can not be applied to the down counter 215, simultaneously the V-RLSA memory 240 enters a write state by the low voltage signal, and the buffer enters an enable state. Thus the low voltage signal is applied to the V-RLSA memory 240, and the comparator 252 enters a disable state, also the selector 254 selects and outputs the system clock signal ϕ_1 which is previously applied to the input terminal (B) thereof. At this time, the up/down counter 261 functions as a down counter.

At initial state of the period that a low voltage signal is outputted from the flip-flop 268, the mono-multivibrator 274 also outputs a low voltage signal by which the buffer 279 enters its output enable state, thereby causing the output signal from the subtracter 273 to be applied to the address generating counter 261. At this time, the multiplier 272 multiplies the counted value "2" from the up/down counter 261 by the offset value "8" from the latch 211 to obtain the product "16" which in turn is subtracted from the address value "17" of the address generating counter 230 by the subtracter 273. As a result,

the subtracter 273 outputs a "1" value signal. At this time, the low voltage pulse signal outputted from the mono-multivibrator 274 is inverted into a high voltage signal by the inverter 276. This high voltage signal is applied via the OR gate 277 to the buffer 273, thereby causing the buffer 273 to enter its output disenable state. Accordingly, "1" value output signal from the subtracter 273 is loaded into the address generating counted 230 via the buffer 279, so that the location of the V-RLSA memory 240 corresponding to the address "1" which is the start address of the V-RLSA memory 240 is addressed. Then, the low voltage signal outputted from the buffer 251 is written into the location corresponding to the address "1".

On the other hand, the system clock signal ϕ_1 is applied via the selector 254 to the up/down counter 261 which in tum counts down said signal, so that the counted value "1" can be obtained.

Thereafter, a "9" value signal outputted from the address 217 is loaded into the address generating counter 230 via the buffer 278, so that the location of the V-RLSA memory 240 corresponding to address "9" which is the second address of the first column of the V-RLSA memory 240 is addressed. As a result, a low voltage signal is written into the location corresponding to the address "9".

At this time, the up/down counter 261 counts down again the system clock signal ϕ_1 as mentioned above, thereby the counted value thereof to be "O" and a low voltage carry signal to be outputted. By the low voltage signal, the AND gate 267 outputs a low voltage signal which clears the up/down counter 261. Also, the AND gate 265 outputs a low voltage signal which presets the flip-flop 268. As a result, the flip-flop 268 outputs a high voltage signal as a read control signal. Thus, a read operation will be carried out, as mentioned above.

That is, locations of the V-RLSA memory 240 are sequentially addressed. The addressing starts at the location corresponding to the address "17". Data read out from the addressed locations is at low voltage state, as shown in the table of Fig. 3A, so that the output signal from the comparator 252 is maintained at the previous state in which low voltage signal is outputted from the output terminal (A=B) and high voltage signal is outputted from the output terminal (A<B). As a result, no system clock signal ϕ_1 is applied to the up/down counter 261, thereby causing the up/down counter 261 to maintain the counted value "O". At this time, the system clock signal ϕ_1 is applied via the AND gate 218 to the down counter 215 which in turn counts down said signal ϕ_1, thereby causing the counted value thereof to be "6".

When data read out from the sequentially-addressed locations of the first column of the V-RLSA memory 240 is maintained at low voltage state, the up/down counter 261 maintains continuously the counted value "O" and the down counter 215 counts down by "1" at a time.

On the other hand, when data read out from the sequentially-addressed locations of the first column of the V-RLSA memory 240 is maintained at high voltage state, output signal from the comparator 252 is inverted. Thereby, the comparator 252 is maintained at a state that the output terminal (A=B) thereof to output a high voltage signal and the output terminal (A<B) thereof to output a low voltage signal. As a result, system clock signal ϕ_1 is applied to the up/down counter 261, thereby the up/down counter 216 to count up from "O", by "1" at a time and the down counter 215 to count down by "1" at a time.

After data has been read out from all (that is, "9") locations corresponding to addresses of the first column of the V-RLSA 240, the counted value from the down counter 215 is "O", thereby causing the down counter 215 to output a low voltage carry signal. By this low voltage signal, the AND gate 262 output a low voltage signal which enables the comparator 263. As a result, the comparator 263 compares the counted value from the up/down counter 261 with the vertical threshold value from the threshold setting unit 264. At this time, when the counted value from the up/down counter 261 is "4" as high voltage state of data is continued 4 times, as shown in the table of Fig. 3A, the comparator 263 outputs a low voltage signal at the output terminal (A<B) thereof and a high voltage signal at the output terminal (A≥B) thereof. At initial state of the period that this high voltage signal is outputted, the mono-multivibrator 266 outputs a low voltage pulse signal, thereby causing the AND gate 267 to output a low voltage signal which clears the up/down counter 261.

The low voltage carry signal outputted from the down counter 215 is also applied as a clock signal to the up counter 212, thereby causing the counted value from the up counter 212 to be incremented by "1". That is, the output signal from the up counter 212 has "2" value. The low voltage carry signal is also applied via the buffer 217 to the AND gate 216, thereby causing the AND gate 216 to output a low voltage signal. As a result, "9" value, the number of vertical pixels latched by the latch 213 is loaded into the down counter 215, on the other hand, "2" value of the output signal from the up counter 212 is loaded into the address generating counter 230 via the buffer 214, so that the location of the V-RLSA memory 240 corresponding to address "2" which is the first address of the second column of the V-RLSA memory 240 is addressed. Subsequent operations are carried out in the same manner as mentioned above.

On the other hand, the low voltage carry signal outputted from the down counter 215 is also applied as a clock signal to the up counter 224 which in turn counts up said clock signal. The counted value from the up counter 224 is compared with "8" value, the offset value from the latch 211, by the comparator 221. When the counted value from the up counter 224 is "8" value as processing for all columns of the V-RLSA 240 has been carried out, the comparator 221 outputs a high voltage signal at the output terminal (A=B) thereof. At initial state

of the period that this high voltage signal is outputted, the mono-multivibrator 222 outputs a low voltage pulse signal which is in turn applied as clock signal to the flip-flop 223. As a result, the flip-flop 223 outputs low voltage signal which is in turn applied to one input terminal of the AND gate 225, so that reference clock signal ϕ can not pass through the AND gate 225, thereby causing the AND gate 225 to input no system clock signal ϕ_1. Thus, the above operation will be finished.

As apparent from the flowchart of Fig. 5, pixel data is read out from the addressed locations of the V-RLSA memory 240, in order to determine its voltage state. When pixel data is at high voltage state, the counted value from the up/down counter 261 is incremented by "1". Then, a location corresponding to the value obtained by adding the offset value from the latch 211 to the current address value is addressed, so that next pixel data is read out. If this pixel data is at low voltage and the previous pixel data is also at low voltage, next pixel data is read out, under the condition that the counted value of the up/down counter 261 maintains "O" value. On the other hand, when only the previous pixel data is at high voltage, the counted value from the up/down counter 261 is compared with the vertical threshold value from the threshold setting unit 264. If the counted value from the up/down counter 261 is not less than the vertical threshold value, next pixel data is read out, under the condition that the counted value from the up/down counter 261 maintains "O" value. If the counted value from the up/down counter 261 is less than the vertical threshold value, the counted value from the up/down counter 261 is multipiled by the offset value from the latch 211. Then, the product is subtracted from the current address value, so that a location of the V-RLSA memory 240 corresponding to the obtained value is addressed. After pixel data read out from the location is maintained at low voltage state, the counted value of the up/down counter 261 is decremented by "1". Then, when the counted value from the up/down counter 261 is not "O", the offset value from the latch 211 is added to the current address value, so that next location of the V-RLSA memory 240 corresponding to the obtained value is addressed. Thereafter, subsequent operations for maintaining pixel data at low voltage state are repeatedly carried out. When the counted value from the up/down counter 261 is "O", next location of the V-RLSA memory 240 is addressed and next pixel is read out from said addressed location, as mentioned above.

By the above operations, vertical pixel data shown in Fig. 3A is smoothed as shown in Fig. 3B.

On the other hand, logical combination of pixel data processed by vertical/horizontal-run length smoothing algorithm processes is carried out by a circuit shown in Fig. 6.

During the period that a horizontal-run length smoothing algorithm process is carried out by the H-RLSA circuit 100, the V-RLSA circuit 200 does not output a low voltage end signal ES, that is, outputs a high voltage signal. As a result, the OR gate 311 outputs continuously high voltage signal, irrespective of reference clock signal ϕ, thereby causing the flip-flop 312 to output no system clock signal ϕ_1.

By the high voltage signal, each of selectors 322 to 325 selects a signal which is inputted to its input terminal A and in turn outputs it.

Accordingly, address signal outputted from the H-RLSA circuit 100 is applied via the selector 322 to the H-RLSA memory 120, so that a location of the H-RLSA memory 120 corresponding to the address signal is addressed. On the other hand, read/write control signals R/W outputted from the H-RLSA circuit 100 are applied via the selector 324 to the H-RLSA memory 120, thereby causing read and write operations of the H-RLSA memory 120 to be controlled.

During the period that a vertical-run length smoothing algorithm process is carried out by the V-RLSA circuit 200, address signal outputted from the V-RLSA circuit 200 is applied via the selector 323 to the V-RLSA memory 240, so that a location of the V-RLSA memory 240 corresponding to the address signal is addressed. Also, read/write control signals R/W outputted from the V-RLSA circuit 200 are applied via the selector 325 to the V-RLSA memory 240, thereby causing read and write operations of the V-RLSA memory 240 to be controlled.

On the other hand, when the vertical-run length smoothing algorithm process is completed, the V-RLSA circuit 200 outputs low voltage end signal ES. This low voltage end signal ES is applied to one input terminal of the OR gate 311, so that reference clock signal O is applied via the OR gate 311 to the flip-flop 312 as a clock signal. As a result, the flip-flop 312 outputs system clock signal O_1 which is in turn applied to the down dounter 314 and the up counter 313 as a count clock signal. The system clock signal O_1 is also applied to the input terminal (B) of the selector 324 and the output enable terminal (OE) of the buffer 340.

By the low voltage end signal ES, each of selectors 322 to 325 selects a signal which is inputtad to its input terminal B and outputs it. The low voltage end signal ES is inverted into a high voltage signal and in turn applied to the input terminal (B) of the selector 324. Accordingly, the up counter 313 counts system clock signal ϕ_1 as shown in Fig. 7B and outputs the counted signal to the H-RLSA memory 120 and the V-RLSA memory 240 via the selectors 322 to 323, respectively. As a result, locations of the H-RLSA memory 120 and the V-RLSA memory 240 corresponding to the counted value are sequentially addressed. At this time, the system clock signal ϕ_1 is applied via the selector 324 to read/write control signals as shown in Fig. 7C, thereby causing the H-RLSA memory 120 to be at its read state during the high voltage period of the system clock signal ϕ_1 and at its write state during the low voltage period of the system clock signal ϕ_1. On the other hand, the high voltage signal applied to the input terminal (B) of the selector 325 is ap-

plied to the V-RLSA memory 240 as a read control signal, as shown in FIG. 7D, thereby causing the V-RLSA memory 240 to be maintained at its read state.

As locations of the H-RLSA memory 120 and the V-RLSA memory 240 corresponding to the same counted value of the up counter 313 are addressed as stated above, the data of the addressed location of the H-RLSA memory 120 is read out during the high voltage period of the system clock signal ϕ_1 and the data of the addressed location of the V-RLSA memory 240 is directly read out, such data which are read out from the addressed locations of the H-RLSA memory 120 and the V-RLSA memory 240 corresponding to the same counting value are ANDed by bit unit at the AND gate 330 and are applied to the buffer 340.

On the other hand, the system clock signal ϕ_1 is applied to the buffer 340 as output enable control signal shown in Fig. 7E, sequentially as the buffer 340 enters the output enable state during the low voltage period of the system clock signal ϕ_1, thus the data which is inputted into the buffer 340 is outputted as shown in Fig. 7F. At this time, as the H-RLSA memory 120 enters write state when the system clock signal ϕ_1 is low voltage signal, the data which is outputted from the buffer 340 is written into the addressed location of the H-RLSA memory 120. Namely, the pixel data of the H-RLSA memory 120 shown in Fig. 8A and the pixel data of the V-RLSA memory 240 shown in Fig. 8B are ANDed and written into the H-RLSA memory 120 as shown in Fig. 8C. On the other hand, the down counter 314 counts down the system clock signal ϕ_1, accordingly when the system clock signal ϕ_1 of the predetermined number of times which is required to complete the performance of the above ANDed combination is outputted, the low voltage carry signal is outputted from the down counter 314 to clear the flip-flop 312, and then no system clock signal ϕ_1 is outputted, thereby the above operation can be completed.

As previously stated above, in accordance with the present invention, the horizontal/vertical-run length smoothing algorithm processes are performed directly by a hardware not by a microprocessor's program, and the data which is performed by the horizontal/vertical-run length smoothing algorithm processes is logical-program. Therefore, the document acknowledge system of the present invention performs tasks much faster than the prior arts do and increases the using efficiency of microprocessors by reducing tasks thereof.

While preferred embodiments of the present invention have been illustrated, it will be understood that those are by way of illustration only, and that various changes and modifications may be made within the contemplation of the invention and within the scope of the claims.

Claims

1. A circuit for performing a horizontal run-length smoothing algorithm (H-RLSA) in a document acknowledge system, comprising memory means (120) for storing digital data of a document and for outputting stored datum in a read mode, wherein the data outputted from the memory means (120) are scanned horizontally in the memory means (120) in order to get a horizontal run-length which represents horizontally adjacent black pixels, characterized in that it comprises:

   address generating means (110) for generating an address of the memory means (120);
   first comparing means (132) for determining whether a data outputted from the memory means (120) represents a black pixel or a white pixel;
   counting means (141) for counting a run-length of data representing adjacent black pixels outputted from the first comparing means (132);
   second comparing means (143) for determining whether the run-length counted by the counting means (141) is smaller than a threshold value;
   clearing means (146) for clearing the counting means (141) when the counted run-length is not smaller than the threshold value;
   write address setting means (150) for setting an address pointer on a first black pixel of the data representing adjacent black pixels when the run-length is smaller than the threshold value; and
   writing means (131) for changing a datum representing a black pixel to a datum representing a white pixel in the memory means when the run-length is smaller than the threshold value.

2. The circuit of claim 1, wherein the first comparing means (132) includes a comparator (132) for comparing the data outputted from the memory means (120) with a reference value (B^+) and applying a clock signal (ϕ_1) to the counting means (141) when the outputted data is equal to the reference value (B^+) and enabling the second comparing means (143) when the outputted data is smaller than the reference value (B^+).

3. The circuit of claim 1 or 2, wherein the counting means includes an up/down counter (141) for counting upwardly a signal inputted from the first comparing means (132) and counting downwardly when the run-length is smaller than the threshold value.

4. The circuit of one of claims 1 to 3, wherein the write address setting means (150) includes a subtractor

(152) for subtracting the run-length from a present address and then inputting a subtracted value to the address generating means (110).

5. The circuit of one of claims 1 to 4, wherein the writing means includes a buffer (131) for applying zero data to the memory means (120) in a writing mode in order to change a datum representing a black pixel to a datum representing a white pixel when the run-length is smaller than the threshold value.

6. A circuit for performing a vertical run-length smoothing algorithm (V-RLSA) in a document acknowledge system, comprising memory means (240) for storing digital data of a document and for outputting a Stored data in a read mode and for changing a stored datum in a write mode, wherein the data outputted from the memory means (240) are scanned vertically in the memory means (240) in order to get a vertical run-length which represents vertically adjacent black pixels, characterized in that it comprises:

start address setting means (210) for generating a start address signal of each column for a vertical scanning of the memory means (240) and for generating a control signal to control following adress in each column;
address generating means (230, 270) for generating an address of the memory means (240) to be accessed or to be written responsive to the control signal from the start address setting means (210) and to the selection of the read mode or the write mode;
first comparing means (252) for determining whether a data outputted from the memory means (240) in the read mode represents a black pixel or a white pixel;
counting means (261) for counting a run-length of data representing adjacent black pixels outputted from the first comparing means (252);
second comparing means (263) for determining whether the run-length counted by the counting means is smaller than a threshold value;
clearing means (266, 267) for clearing the counting means (261) when the counted run-length is not smaller than the threshold value as a result of the second comparing means (263);
write address setting means (272, 273) for setting an address pointer on a first black pixel of the data representing adjacent black pixels in the write mode when the run-length is smaller than the threshold value as a compared result from the second comparing means (263); and
writing means (251) for changing a datum representing a black pixel to a datum representing a white pixel in the memory means (240) in the write mode when the run-length is smaller than the threshold value as determined by the second comparing means, timing operation of the aforesaid means being in accordance with a system clock signal.

7. The circuit of claim 6, wherein the first comparing means includes a comparator (252) for comparing the data outputted from the memory means (240) with a reference value (B^+) and applying a clock signal to the counting means (261) when the outputted data is equal to the reference value (B^+) and enabling the second comparing means (263) when the outputted data is smaller than the reference value (B^+).

8. The circuit of claim 6 or 7, wherein the counting means includes an up/down counter (261) for counting upwardly a signal inputted from the first comparing means (252) and counting downwardly when the run-length is smaller than the threshold value.

9. The circuit of one of claims 6 to 8, wherein the writing means includes a buffer (251) for applying zero data to the memory means (240) in a writing mode in order to change a datum representing a black pixel to a datum representing a white pixel when the run-length is smaller than the threshold value.

10. The circuit of one of claims 6 to 9, wherein the address setting means, include:

a first latch (211) for latching a number of columns of the document which are to be accessed horizontally;
a second latch (213) for latching a number of rows of the document which are to be accessed vertically;
a down counter (215) for loading the number of rows which are to be accessed from the second latch (213) and for, responsive to the system clock signal and selection of the read/write mode, counting down the loaded number of rows to output a carry signal when the counted value becomes zero;
a first up-counter (212) for, responsive to the carry signal, counitng the start address signal of columns which are to be accesssed for the vertical scanning of the memory means (240) and for outputting the counted start address signal to the address generating means (230, 270);
a control signal generating means (217, 216) for outputting a control signal to the address generating means (230, 270) responsive to the carry signal from the down counter (215) in or-

der to control a provision of the start signal to the address generating means (230, 270);
a second up counter for counting the number of columns which are to be accessed responsive to the carry signal from the down counter (215);
a comparator (221) for comparing the number of the columns to be accessed from the first latch (211) and the number of the columns accessed from the second up counter; and
a flip-flop (223) for controlling a provision of the system clock signal responsive to a comparison result from the comparator(221).

11. A circuit according to one of claims 6 to 10, wherein the address generating means include:

an address generating counter (230) for outputting a start address of each column for the vertical scanning upon receiving the start address from the start address setting means (210) and outputting following addresses to be accessed and to be written in each column after outputting the start address;
an adder (271) for adding output signals from the generating counter (230) and the first latch (211) and for outputting an added value to the address generating counter (230); and
an OR gate to control a provision of the added value to the address generating counter (230) responsive to the control signal from the control signal generating means (216, 217), the system clock signal, and the compared result from the second comparing means (263).

12. A circuit for performing a horizontal run-length smoothing algorithm 'H-RLSA' and a vertical run-length smoothing algorithm 'V-RLSA' in a document acknowledge system, and for combining the outputs of said H-RLSA and V-RLSA algorithm by ANDing the resulting outputs, characterized in that it comprises:

a H-RLSA circuit (100, 120) for performing a horizontal run-length smoothing algorithm (H-RLSA) according to one of claims 1 to 5;
a V-RLSA circuit (200, 240) for performing a vertical run-length smoothing algorithm (V-RLSA) according to one of claims 6 to 11, said V-RLSA circuit (200, 240) further comprising means for providing an end signal indicating that an operation of said V-RLSA circuit is completed;
a system clock and address supplying unit (310) for supplying a system clock signal (ϕ_1) in response to said end signal of said V-RLSA circuit (200, 240), counting the system clock signal to output the counted value as horizontal/vertical address of the memories (120, 240) to be accessed, wherein the horizontal/vertical address designates a same pixel location of the memories (120, 240), and stopping supplying the system clock signal when the system clock signal has been outputted therefrom a predetermined number of times;
an address and read/write selecting unit (320) for selecting a read/write control signal and an address signal from the H-RLSA circuit (100) and the V-RLSA circuit (200) respectively and outputting the read/write control signal and the address signal into the H-RLSA memory (120) and the V-RLSA memory (240) respectively in response to the output signals from the system clock and address supplying unit (310);
an AND gate (330) for ANDing output data from said memory means (120, 240) of said H-RLSA and V-RLSA circuits to each pixel location;
a buffer (340) for allowing an output signal from said AND gate (330) to be passed therethrough during a half cycle of the system clock signal (ϕ_1) to apply the output signal from said AND gate (330) as write data to the memory means (120) of said H-RLSA circuit.

13. A circuit according to claim 12, characterized in that said system clock and address supplying unit (310) comprises an OR gate (311) for ORing the end signal of said V-RLSA circuit and a reference clock signal (ϕ), a flip-flop (312) for inputting an output signal from said OR gates as the system clock signal (ϕ_1), an up counter (313) for counting up the system clock signal (ϕ_1) to output the counted value as the horizontal/vertical address, and a down counter (314) for counting down the system clock signal (ϕ_1) a predetermined number of times to generate a carry signal to apply the carry signal as a clear signal to said flip-flop (312).

14. A circuit according to claim 12 or 13, wherein said address and read/write selecting unit (320) comprises:

an inverter for inverting (221) the end signal of said V-RLSA circuit;
a selector (322) responsive to the end signal of said V-RLSA circuit for selecting one of a horizontal address signal of said H-RLSA circuit and the counted value from said system clock and address supplying unit (310) to output the selected signal as a horizontal address signal;
a selector (323) responsive to the end signal of said V-RLSA circuit for selecting one of a vertical address signal of said V-RLSA circuit and the counted value from said system clock and address supplying unit (310) to output the selected signal as a vertical address signal;

a selector (324) responsive to the end signal of said V-RLSA circuit for selecting one of horizontal read/write control signals of said H-RLSA circuit and the system clock signal (ϕ_1) to output the selected signal as a horizontal read/write control signal; and
a selector (325) responsive to the end signal of said V-RLSA circuit and an output signal of said inverter (221) to output the selected signal as a vertical read/write control signal.

Patentansprüche

1. Eine Schaltung zur Anwendung eines horizontalen Lauflängeglättungsalgorithmusses (H-RLSA) in einem Vorlagenerkennungssystem, das eine Speichervorrichtung (120) umfaßt, in der die digitalen Daten einer Vorlage gespeichert werden und welche die Ausgabe der gespeicherten Daten in einem Lesemodus ermöglicht, wobei die durch die Speichervorrichtung (120) ausgegebenen Daten in der Speichervorrichtung (120) horizontal gescanned werden, um eine horizontale Lauflänge zu ermitteln, die horizontal aneinander angrenzende schwarze Pixel repräsentiert, wobei die Schaltung durch folgende Komponenten gekennzeichnet ist:

   Adressenerstellungsvorrichtung (110) zur Erzeugung einer in der Speichervorrichtung (120) gespeicherten Adresse;

   erste Vergleichsvorrichtung (132) die dazu dient, zu ermitteln, ob ein von der Speichervorrichtung (120) ausgegebener Datenwert einen schwarzen Pixel oder einen weißen Pixel repräsentiert;

   Zählvorrichtung (141) zur Zählung der Anzahl einzelner, von der ersten Vergleichsvorrichtung (132) ausgegebener Datenwerte, die aneinander angrenzende schwarze Pixel repräsentieren und zusammen eine bestimmte Lauflänge ergeben;

   zweite Vergleichsvorrichtung (143), die dazu dient, zu ermitteln, ob die durch die Zählvorrichtung (141) ermittelte Lauflänge kleiner ist als ein festgelegter Schwellenwert;

   Löschvorrichtung (146) zum Löschen des durch die Zählvorrichtung (141) ermittelten Wertes, wenn die festgestellte Lauflänge nicht kleiner ist als der Schwellenwert;

   Adressenschreibpositionierungsvorrichtung (150) zur Positionierung eines Adressenzeigers auf den ersten schwarzen Pixel der Daten, die aneinander angrenzende schwarze Pixel repräsentieren, wenn die Lauflänge kleiner ist als der Schwellenwert; und

   Schreibvorrichtung (131) zur Änderung eines Datenwertes, der einen schwarzen Pixel repräsentiert, in einen Datenwert, der einen weißen Pixel repräsentiert in der Speichervorrichtung, wenn die Lauflänge kleiner ist als der Schwellenwert.

2. Die Schaltung nach Schutzanspruch 1, dadurch gekennzeichnet, daß die erste Vergleichsvorrichtung (132) einen Vergleicher (132) beinhaltet, der dazu dient, die von der Speichervorrichtung (120) ausgegebenen Daten mit einem Referenzwert (B+) zu vergleichen und in der Zählvorrichtung (141) ein Taktsignal (ϕ1) auszulösen, wenn der ausgegebene Datenwert dem Referenzwert (B+) entspricht, sowie dazu, die zweite Vergleichsvorrichtung (143) zu aktivieren, wenn der ausgegebene Datenwert kleiner ist als der der Referenzwert (B+).

3. Die Schaltung nach Schutzanspruch 1 oder 2, dadurch gekennzeichnet, daß die Zählvorrichtung einen Aufwärts-/Abwärtszähler (141) umfaßt, der dazu dient, aufwärts zu zählen, wenn ein Signal von der ersten Vergleichsvorrichtung (132) eingegeben wird und abwärts zu zählen, wenn die Lauflänge kleiner ist als der Schwellenwert.

4. Die Schaltung nach einem der Schutzansprüche 1 bis 3, dadurch gekennzeichnet, daß die Adressenschreibpositionierungsvorrichtung (150) einen Subtraktor (152) umfaßt, der dazu dient, die Lauflänge von einer vorhandenen Adresse zu subtrahieren und dann den subtrahierten Wert in die Adressenerstellungsvorrichtung (110) einzugeben.

5. Die Schaltung nach einem der Schutzansprüche 1 bis 4, dadurch gekennzeichnet, daß die Schreibvorrichtung einen Pufferspeicher (131) beinhaltet, dessen Aufgabe es ist, in einem Schreibmodus einen Datenwert Null an die Speichervorrichtung (120) zu übermitteln, um einen Datenwert, der einen schwarzen Pixel repräsentiert, in einen Datenwert zu ändern, der einen weißen Pixel repräsentiert, wenn die Lauflänge kleiner ist als der Schwellenwert.

6. Eine Schaltung zur Anwendung eines vertikalen Lauflängeglättungsalgorithmusses (V-RLSA) in einem Vorlagenerkennungssystem, die eine Speichervorrichtung (240) umfaßt, in der die digitalen Daten einer Vorlage gespeichert werden und die die Ausgabe der gespeicherten Daten in einem Lesemodus ermöglicht, und die die Änderung der gespeicherten Daten in einem Schreibmodus ermög-

licht, wobei die durch die Speichervorrichtung (240) ausgegebenen Daten in der Speichervorrichtung (240) vertikal gescanned werden, um eine vertikale Lauflänge zu ermitteln, die vertikal aneinander angrenzende schwarze Pixel repräsentiert, wobei die Schaltung durch folgende Komponenten gekennzeichnet ist:

Adressenpositionierungsstartvorrichtung (210) zur Erzeugung eines Adressenstartsignals in jeder Spalte für ein vertikales Scanning der Speichervorrichtung (240) und zur Erzeugung eines Steuersignals für die richtige Positionierung der folgenden Adresse in der jeweiligen Spalte;

Adressenerstellungsvorrichtung (230, 270) zur Erzeugung einer in der Speichervorrichtung (240) gespeicherten Adresse, die in Abhängigkeit vom durch die Adressenpositionierungsstartvorrichtung (210) abgegebenen Steuersignal und abhängig davon, ob der Lese- oder der Schreibmodus ausgewählt wurde, gelesen oder geschrieben werden kann;

erste Vergleichsvorrichtung (252), die dazu dient, zu ermitteln, ob ein von der Speichervorrichtung (240) im Lesemodus ausgegebener Datenwert einen schwarzen Pixel oder einen weißen Pixel repräsentiert;

Zählvorrichtung (261) zur Zählung der Anzahl einzelner, von der ersten Vergleichsvorrichtung (252) ausgegebener Datenwerte, die aneinander angrenzende schwarze Pixel repräsentieren und zusammen eine bestimmte Lauflänge ergeben;

zweite Vergleichsvorrichtung (263), die dazu dient, zu ermitteln, ob die durch die Zählvorrichtung (141) ermittelte Lauflänge kleiner ist als ein festgelegter Schwellenwert;

Löschvorrichtung (266, 267) zum Löschen des durch die Zählvorrichtung (261) ermittelten Wertes, wenn die durch die zweite Vergleichsvorrichtung (263) festgestellte Lauflänge nicht kleiner ist als der Schwellenwert;

Adressenschreibpositionierungsvorrichtung (272, 273) zur Positionierung eines Adressenzeigers auf den ersten schwarzen Pixel der Daten, die im Schreibmodus aneinander angrenzende schwarze Pixel repräsentieren, wenn die Lauflänge gemäß des durch die zweite Vergleichsvorrichtung (263) ermittelten Vergleichswertes kleiner ist als der Schwellenwert; und

Schreibvorrichtung (251) zur Änderung eines Datenwertes, der einen schwarzen Pixel repräsentiert, in einen Datenwert, der einen weißen Pixel repräsentiert, in der Speichervorrichtung (240) im Schreibmodus, wenn die Lauflänge kleiner ist als der durch die zweite Vergleichsvorrichtung ermittelte Schwellenwert, die Zeitsteuerung für die vorstehend beschriebene Vorrichtung erfolgt über ein vom System generiertes Taktsignal.

7. Schaltung nach Schutzanspruch 6, dadurch gekennzeichnet, daß die erste Vergleichsvorrichtung einen Vergleicher (252) beinhaltet, der dazu dient, die von der Speichervorrichtung (240) ausgegebenen Daten mit einem Referenzwert (B+) zu vergleichen und in der Zählvorrichtung (261) ein Taktsignal auszulösen, wenn der ausgegebene Datenwert dem Referenzwert (B+) entspricht, sowie dazu, die zweite Vergleichsvorrichtung (263) zu aktivieren, wenn der ausgegebene Datenwert kleiner ist als der der Referenzwert (B+).

8. Die Schaltung nach Schutzanspruch 6 oder 7, dadurch gekennzeichnet, daß die Zählvorrichtung einen Aufwärts-/Abwärtszähler (261) umfaßt, der dazu dient, aufwärts zu zählen, wenn ein Signal von der ersten Vergleichsvorrichtung (252) eingegeben wird und abwärts zu zählen, wenn die Lauflänge kleiner ist als der Schwellenwert.

9. Die Schaltung nach einem der Schutzansprüche 6 bis 8, dadurch gekennzeichnet, daß die Schreibvorrichtung einen Pufferspeicher (251) beinhaltet, dessen Aufgabe es ist, in einem Schreibmodus einen Datenwert Null an die Speichervorrichtung (240) zu übermitteln, um einen Datenwert, der einen schwarzen Pixel repräsentiert, in einen Datenwert zu ändern, der einen weißen Pixel repräsentiert, wenn die Lauflänge kleiner ist als der Schwellenwert.

10. Die Schaltung nach einem der Schutzansprüche 6 bis 9, wobei die Adressenpositionierungsvorrichtung durch folgende Komponenten gekennzeichnet ist:

einen ersten Signalspeicher (211) zur Speicherung einer bestimmten Anzahl von Spalten der Vorlage, auf die horizontal zugegriffen werden soll;

einen zweiten Signalspeicher (213) zur Speicherung einer bestimmten Anzahl von Zeilen der Vorlage, auf die vertikal zugegriffen werden soll;

einen Abwärtszähler (215), der dazu dient, die

Anzahl der Zeilen zu laden, auf die vom zweiten Signalspeicher (213) aus zugegriffen werden soll und dazu - in Abhängigkeit vom Taktsignal des Systems und von der Auswahl des Schreib-/ oder Lesemodus - die geladene Anzahl von Zeilen abwärts zu zählen und bei Erreichen des Wertes Null ein Übertragssignal zu erzeugen;

einen ersten Aufwärtszähler (212), der dazu dient, in Abhängigkeit vom Übertragssignal das Adressenstartsignal für die Anzahl von Spalten zu zählen, auf die für das vertikale Scanning der Speichervorrichtung (240) zugegriffen werden soll, sowie dazu, das gezählte Adressenstartsignal an die Adressenerstellungsvorrichtung (230, 270) auszugeben;

eine Steuersignalerzeugungsvorrichtung (217, 216) zur Ausgabe eines Steuersignals an die Adressenerstellungsvorrichtung (230, 270) in Abhängigkeit von dem durch den Abwärtszähler (215) erzeugten Übertragssignal, um die Abgabe des Startsignals an die Adressenerstellungsvorrichtung (230, 270) zu steuern;

einen zweiten Aufwärtszähler zur Zählung der Anzahl von Spalten, auf die in Abhängigkeit von dem durch den Abwärtszähler (215) erzeugten Übertragssignal zugegriffen werden soll;

einen Vergleicher (221) zum Vergleich der Anzahl von Spalten, auf die vom ersten Signalspeicher (211) aus zugegriffen werden soll, mit der Anzahl der Spalten, auf die vom zweiten Aufwärtszähler aus zugegriffen werden soll; und

einen Flipflop (223) zur Steuerung der Abgabe des Systemtaktsignals in Abhängigkeit von dem durch den Vergleicher (221) ermittelten Vergleichswert.

11. Die Schaltung nach einem der Schutzansprüche 6 bis 10, wobei die Adressenerstellungsvorrichtung durch folgende Komponenten gekennzeichnet ist:

einen Adreßerstellungszähler (230) zur Ausgabe einer Startadresse für jede Spalte zum vertikalen Scanning nach Empfang der Startadresse von der Adressenpositionierungsstartvorrichtung (210) und zur Ausgabe der folgenden Adressen, die nach Ausgabe der Startadresse in jeder Spalte geschrieben werden sollen oder auf die zugegriffen werden soll;

ein Addierwerk (271) zum Hinzuaddieren von Ausgabesignalen vom Adreßerstellungszähler (230) und vom ersten Signalspeicher (211), sowie zur Ausgabe eines addierten Wertes an den Adreßerstellungszähler (230); und

ein ODER-Gatter zur Steuerung der Weiterleitung des addierten Wertes an den Adreßerstellungszähler (230) in Abhängigkeit von dem durch die Steuersignalerzeugungsvorrichtung (216, 217) abgegebenen Steuersignal, vom Taktsignal des Systems, und vom durch die zweite Vergleichsvorrichtung (263) ermittelten Vergleichswert.

12. Eine Schaltung zur Anwendung eines horizontalen Lauflängeglättungsalgorithmusses (H-RLSA) und eines vertikalen Lauflängeglättungsalgorithmusses (V-RLSA) in einem Vorlagenerkennungssystem und zur Kombinierung der Ausgabewerte der besagten H-RLSA- und V-RLSA-Algorithmen durch Hinzufügen der resultierenden Ausgabewerte, wobei diese Schaltung durch die folgenden Komponenten gekennzeichnet ist:

eine H-RLSA Schaltung (100, 120) zur Anwendung eines horizontalen Lauflängeglättungsalgorithmusses (H-RLSA) nach einem der Schutzansprüche 1 bis 5;

eine V-RLSA Schaltung (200, 240) zur Anwendung eines vertikalen Lauflängeglättungsalgorithmusses (V-RLSA) nach einem der Schutzansprüche 6 bis 11, wobei die besagte V-RLSA-Schaltung (200, 240) zudem Vorrichtungen umfaßt, die dazu dienen, ein Endsignal abzugeben, durch das angezeigt wird, das ein Arbeitsgang der besagten V-RLSA-Schaltung abgeschlossen ist;

eine Systemuhr-/Adreßzuführungseinheit (310) zur Lieferung eines Taktsignals ($\Phi 1$) in Abhängigkeit von besagtem Endsignal, das von der beschriebenen V-RLSA-Schaltung (200, 240) abgegeben wird, wobei diese Einheit das Systemtaktsignal auszählt, um den gezählten Wert dann als horizontale/vertikale Adresse der Speicher (120, 240) auszugeben, auf die zugegriffen werden soll, wobei diese horizontale/vertikale Adresse eine gemeinsame Pixelposition der Speicher (120, 240) bezeichnet und die Abgabe des Systemtaktsignals gestoppt wird, wenn dieses eine vorher festgelegte Anzahl von Malen abgegeben wurde;

eine Adressen- und Lese-/Schreib-Auswahleinheit (320) zur Auswahl eines Lese-/Schreib-Steuersignals und eines Adressensignals von der H-RLSA-Schaltung (100) bzw. der V-RLSA-Schaltung (200) und zur Ausgabe des Lese-/

Schreib-Steuersignals und des Adressensignals in den H-RLSA-Speicher (120) bzw. den V-RLSA-Speicher (240) in Abhängigkeit von den durch die Systemuhr-/Adreßzuführungseinheit (310) erzeugten Signalen;

ein UND-Gatter (330) zum Hinzufügen der Ausgabedaten der besagten, den beschriebenen H-RLSA- und V-RLSA-Schaltungen zugeordneten Speichervorrichtungen (120, 240) zu jeder Pixelposition;

einen Pufferspeicher (340), der es ermöglicht, ein Ausgangssignal von besagtem UND-Gatter (330) während der Dauer eines Halbzyklusses des Systemtaktsignals (Φ 1) durch dieses UND-Gatter zu leiten, um dieses Ausgangssignal des UND-Gatters (330) als Schreibdaten in die Speichervorrichtung (120) der H-RLSA-Schaltung einzulesen.

13. Eine Schaltung nach Schutzanspruch 12, die dadurch gekennzeichnet ist, daß die beschriebene Systemuhr-/Adreßzuführungseinheit (310) folgendes beinhaltet: ein ODER-Gatter (311), das dazu dient, die alternative Anwendung (ORing) des von der V-RLSA-Schaltung erzeugten Endsignals oder des Referenztaktsignals (Φ) zu ermöglichen; ein Flipflop (312) zur Eingabe eines Ausgangssignals von den besagten ODER-Gattern als Systemtaktsignal (Φ1); einen Aufwärtszähler (313) zum Aufwärtszählen des Systemtaktsignals (Φ1) und zur Ausgabe des durch die Zählung ermittelten Wertes als horizontale/vertikale Adresse; und einen Abwärtszähler (314), der dazu dient, das Systemtaktsignal (Φ1) eine vordefinierte Anzahl von Malen herunterzuzählen, um ein Übertragssignal zu erzeugen, das als eindeutiges Signal an den besagten Flipflop (312) übermittelt werden kann.

14. Eine Schaltung nach Schutzanspruch 12 oder 13, bei der die beschriebene Adressen- und Lese-/Schreib-Auswahleinheit (320) durch folgende Komponenten gekennzeichnet ist:

einen Inverter (221) zur Realisierung der Negation des durch die V-RLSA-Schaltung abgegebenen Endsignals;

einen Selektor (322), der in Abhängigkeit von dem durch die V-RLSA-Schaltung abgegebenen Endsignal ein horizontales Adressensignal der H-RLSA-Schaltung und den durch die Systemuhr-/Adreßzuführungseinheit (310) gezählten Wert auswählt, um das ausgewählte Signal als horizontales Adressensignal auszugeben;

einen Selektor (323), der in Abhängigkeit von dem durch die V-RLSA-Schaltung abgegebenen Endsignal ein vertikales Adressensignal der V-RLSA-Schaltung und den durch die Systemuhr-/Adreßzuführungseinheit (310) gezählten Wert auswählt, um das ausgewählte Signal als vertikales Adressensignal auszugeben;

einen Selektor (324), der in Abhängigkeit von dem durch die V-RLSA-Schaltung abgegebenen Endsignal ein horizontales Lese-/Schreib-Steuersignal der H-RLSA-Schaltung und das Systemtaktsignal (Φ1) auswählt, um das ausgewählte Signal als horizontales Lese-/Schreib-Steuersignal auszugeben; und

einen Selektor (325), der in Abhängigkeit von dem durch die V-RLSA-Schaltung abgegebenen Endsignal und einem Ausgangssignal des besagten Inverters (221) arbeitet und dazu dient, das ausgewählte Signal als vertikales Lese-/Schreib-Steuersignal auszugeben.

Revendications

1. Un circuit pour la mise en oeuvre d'un algorithme de lissage par longueur de plage horizontale (H-RLSA) dans un système de reconnaissance de document, comprenant des moyens de mémoire (120) pour le stockage des données numériques concernant un document et pour fournir en sortie, en mode lecture, une donnée stockée, dans lequel les données fournies en sortie des moyens de mémoire (120) sont balayées horizontalement dans les moyens de mémoire (120) pour obtenir une longueur de plage horizontale représentant des pixels noirs adjacents dans le sens horizontal, caractérisé en ce qu'il comprend :

- des moyens de génération d'adresses (110) pour générer une adresse des moyens de mémoire (120);
- des premiers moyens de comparaison (132) pour déterminer si une donnée fournie en sortie des moyens de mémoire (120) représente un pixel noir ou un pixel blanc;
- des moyens de comptage (141) pour compter la longueur de plage des données représentant des pixels noirs adjacents fournies en sortie par les premiers moyens de comparaison (132);
- des deuxièmes moyens de comparaison (143) pour déterminer si la longueur de plage comptée par les moyens de comptage (141) est inférieure à une valeur de seuil;
- des moyens de remise à zéro (146) pour remettre à zéro les moyens de comptage (141) quand

la longueur de plage comptée n'est pas inférieure à la valeur de seuil;

- des moyens de réglage d'adresse d'écriture (150) pour faire régler un pointeur d'adresse sur un premier pixel noir des données représentant des pixels noirs adjacents dans le cas où la longueur de plage est inférieure à la valeur de seuil; et
- des moyens d'écriture (131) pour transformer une donnée représentant un pixel noir en une donnée représentant un pixel blanc dans les moyens de mémoire quand la longueur de plage est inférieure à la valeur de seuil.

2. Le circuit de la revendication 1, dans lequel les premiers moyens de comparaison (132) comprennent un comparateur (132) pour comparer la donnée fournie en sortie par les moyens de mémoire (120) avec une valeur de référence (B^+) et pour appliquer un signal d'horloge (ϕ_1) aux moyens de comptage (141) quand la donnée fournie en sortie est égale à la valeur de référence (B^+) et pour valider les deuxièmes moyens de comparaison (143) quand la donnée fournie en sortie est inférieure à la valeur de référence (B^+).

3. Le circuit de la revendication 1 ou 2, dans lequel les moyens de comptage comprennent un compteur/décompteur (141) pour incrémenter un signal fourni en entrée à partir des premiers moyens de comparaison (132) et pour le décrémenter quand la longueur de plage est inférieure à la valeur de seuil.

4. Le circuit selon l'une des revendications 1 à 3, dans lequel les moyens de réglage de l'adresse d'écriture (150) comprennent un soustracteur (152) pour soustraire la longueur de plage de l'adresse courante et pour fournir ensuite une valeur soustraite en entrée des moyens de génération d'adresse (110).

5. Le circuit selon l'une des revendications 1 à 4, dans lequel les moyens d'écriture comprennent une mémoire tampon (131) pour appliquer des données d'une valeur de zéro aux moyens de mémoire (120) en un mode écriture, afin de transformée une donnée représentant un pixel noir en une donnée représentant un pixel blanc dans le cas où la longueur de plage est inférieure à la valeur de seuil.

6. Un circuit pour mettre en oeuvre un algorithme de lissage par longueur de plage verticale (V-RLSA) dans un système de reconnaissance de document, comprenant des moyens de mémoire (240) pour stocker des données numériques concernant un document et pour fournir en sortie, en mode de lecture, une donnée stockée et pour faire varier une donnée stockée en mode d'écriture, dans lequel les données fournies en sortie des moyens de mémoire (240) sont balayées verticalement dans les moyens de mémoire (240) afin d'obtenir une longueur de plage verticale qui représente des pixels noirs qui sont adjacents dans le sens vertical, caractérisé en ce qu'il comprend :

- des moyens de réglage d'une adresse de début (210) pour générer un signal d'adresse de début pour chaque colonne, pour un balayage vertical des moyens de mémoire (240) et pour générer un signal de commande pour déterminer l'adresse suivante dans chaque colonne :
- des moyens de génération d'adresse (230, 270) pour générer une adresse des moyens de mémoire (240) pour un accès en lecture ou en écriture en fonction du signal de commande reçu des moyens de réglage d'adresse de début (210) et en fonction du choix du mode de lecture ou du mode d'écriture;
- des premiers moyens de comparaison (252) pour déterminer si une donnée fournie en sortie des moyens de mémoire (240) en mode lecture représente un pixel noir ou un pixel blanc;
- des moyens de comptage (261) pour compter la longueur de plage de données représentant des pixels noirs adjacents fournis en sortie par lesdits premiers moyens de comparaison (252);
- des deuxièmes moyens de comparaison (263) pour déterminer si la longueur de plage comptée par les moyens de comptage est inférieure à une valeur seuil;
- des moyens de remise à zéro (266, 267) pour remettre à zéro les moyens de comptage (261) dans le cas où la longueur de plage comptée n'est pas inférieure à la valeur de seuil, en fonction du résultat des deuxièmes moyens de comparaison (263);
- des moyens de réglage d'adresse d'écriture (272, 273) pour régler un pointeur d'adresse sur un premier pixel noir des données représentant des pixels noirs adjacents en mode écriture dans le cas où la longueur de plage est inférieure à la valeur de seuil, en tant que résultat de comparaison dans les deuxièmes moyens de comparaison (263); et
- des moyens d'écriture (251) pour transformer une donnée représentant un pixel noir en une donnée représentant un pixel blanc dans les moyens de mémoire (240) en mode écriture quand la longueur de plage est inférieure à la valeur de seuil, tel que déterminé par les deuxièmes moyens de comparaison, le fonctionnement desdits moyens précités étant synchronisé avec un signal d'horloge système.

7. Le circuit selon la revendication 6, dans lequel les

premiers moyens de comparaison comprennent un comparateur (252) pour comparer la donnée fournie en sortie par les moyens de mémoire (240) avec une valeur de référence (B^+) et pour appliquer un signal d'horloge aux moyens de comptage (261) dans le cas où la donnée fournie en sortie est égale à la valeur de référence (B^+) et pour valider les deuxièmes moyens de comparaison (263) dans le cas où la donnée fournie en sortie est inférieure à la valeur de référence (B^+).

8. Le circuit de la revendication 6 ou 7, dans lequel les moyens de comptage comprennent un compteur/décompteur (261) pour incrémenter un signal fourni en entrée à partir des premiers moyens de comparaison (252) et pour le décrémenter dans le cas où la longueur de plage est inférieure à la valeur de seuil.

9. Le circuit selon l'une des revendications 6 à 8, dans lequel les moyens d'écriture comprennent une mémoire tampon (251) pour appliquer une donnée de zéro aux moyens de mémoire (240) selon un mode d'écriture afin de transformer une donnée représentant un pixel noir en une donnée représentant un pixel blanc dans le cas où la longueur de plage est inférieure à la valeur de seuil.

10. Le circuit selon l'une des revendications 6 à 9, dans lequel les moyens de réglage d'adresse comprennent :

- un premier registre de verrouillage (211) pour verrouiller un nombre de colonnes du document auxquelles il faut accéder horizontalement;
- un registre de verrouillage (213) pour verrouiller un nombre de lignes du document auxquelles il faut accéder verticalement;
- un décompteur (215) pour charger le nombre de lignes auxquelles il faut accéder à partir du deuxième registre de verrouillage (213) et pour, en réponse au signal d'horloge système, et à la sélection du mode lecture/écriture, décrémenter le nombre de lignes chargées pour fournir en sortie un signal de retenue dans le cas où la valeur comptée devient égale à zéro;
- un premier compteur (212) destiné à incrémenter, en réponse au signal de retenue, le signal d'adresse de début des colonnes auxquelles il faut accéder pour le balayage vertical des moyens de mémoire (240) et pour fournir en sortie le signal d'adresse de début ainsi incrémenté à des moyens de génération d'adresse (230, 270);
- des moyens de génération de signal de commande (217, 216) pour fournir en sortie un signal de commande vers les moyens de génération d'adresse (230, 270) en réponse au signal de retenue du décompteur (215) pour commander l'envoi d'un signal de début aux moyens de génération d'adresse (230, 270);
- un deuxième compteur pour compter le nombre de colonnes auxquelles il faut accéder en réponse au signal de retenue fourni par le décompteur (215);
- un comparateur (221) pour comparer le nombre de colonnes auxquelles il faut accéder à partir du premier registre à verrouillage (221) ainsi que le nombre de colonnes auxquelles il faut accéder à partir du deuxième compteur; et
- une bascule (223) pour contrôler l'émission d'un signal d'horloge système en réponse au résultat de la comparaison du comparateur (221).

11. Un circuit selon l'une des revendications 6 à 10, dans lequel les moyens de génération d'adresse comprennent :

- un compteur de génération d'adresse (230) pour fournir en sortie l'adresse de début de chaque colonne pour le balayage vertical, suite à la réception de l'adresse de début à partir des moyens de réglage de l'adresse de début (210) et pour fournir en sortie les adresses suivantes auxquelles il faut accéder et dans lesquelles il faut écrire dans chaque colonne, après avoir fourni en sortie l'adresse de début;
- un additionneur (271) pour additionner des signaux de sortie du compteur de génération d'adresse (230) et du premier registre à verrouillage (211) et pour fournir en sortie la somme au compteur de génération d'adresse (230) : et
- une porte OU pour contrôler l'envoi de la somme au compteur de génération d'adresse (230) en réponse au signal de commande fourni par les moyens de génération de signal de commande (216, 217), au signal d'horloge-système et du résultat de comparaison des deuxièmes moyens de comparaison (263).

12. Un circuit pour mettre en oeuvre un algorithme de lissage par longueur de plage horizontale H-RLSA ainsi qu'un algorithme de lissage par longueur de plage verticale V-RLSA dans un système de reconnaissance de document, et pour combiner les sorties desdits algorithmes H-RLSA et V-RLSA au moyen d'une opération logique ET sur les sorties résultantes, caractérisé en ce qu'il comprend :

- un circuit H-RLSA (100, 120) pour mettre en oeuvre un algorithme de lissage par longueur de plage horizontale (H-RLSA) selon l'une des revendications 1 à 5;

- un circuit V-RLSA (200, 240) pour mettre en oeuvre un algorithme de lissage par longueur de plage verticale (V-RLSA) selon l'une des revendications 6 à 11, ledit circuit V-RLSA (200, 240) comprenant en outre des moyens permettant de fournir un signal de fin indiquant qu'une opération dudit circuit V-RLSA est terminée;
- une unité fournissant un signal d'horloge système ainsi que des adresses (310), pour fournir un signal d'horloge système (ϕ_1) en réponse audit signal de fin dudit circuit VRLSA (200, 240) et pour incrémenter le signal d'horloge système afin de fournir en sortie la valeur incrémentée en tant qu'adresse horizontale/verticale des mémoires (120, 240) auxquelles il faut accéder, dans lequel l'adresse horizontale/verticale désigne un même emplacement de pixel des mémoires (120, 240), et pour arrêter l'émission du signal d'horloge système suite à l'émission par cette unité du signal d'horloge système un nombre prédéterminé de fois;
- une unité de sélection d'adresse et de lecture/écriture (320) destinée à sélectionner un signal de commande de lecture/écriture ainsi qu'un signal d'adresse à partir, respectivement, du circuit H-RLSA (100) et du circuit V-RLSA (200) et pour fournir en sortie le signal de commande de lecture/écriture ainsi que le signal d'adresse à la mémoire H-RLSA (120) et la mémoire V-RLSA (240), respectivement, en réponse aux signaux de sortie de ladite unité fournissant le signal d'horloge système et les adresses (310);
- une porte ET (330) pour réaliser une opération logique ET sur les données de sortie desdits moyens de mémoire (120, 240) desdits circuits H-RLSA et V-RLSA pour chaque emplacement de pixel;
- une mémoire tampon (340) permettant le passage d'un signal de sortie provenant de ladite porte ET (330) pendant un demi-cycle dudit signal d'horloge système afin d'appliquer le signal de sortie de ladite porte ET (330) en tant que donnée d'écriture aux moyens de mémoire (120) dudit circuit H-RLSA.

13. Un circuit selon la revendication 12, caractérisé en ce que ladite unité fournissant le signal d'horloge système et des adresses (310) comprend une porte OU (311) pour effectuer une opération logique OU sur le signal de fin dudit circuit V-RLSA et sur le signal d'horloge de référence (ϕ), une bascule (312) pour fournir en entrée un signal de sortie desdites portes OU en tant que signal d'horloge système (ϕ_1), un compteur (313) pour compter le signal d'horloge système (ϕ_1) afin de sortir la valeur de comptage en tant qu'adresse horizontale/verticale ainsi qu'un décompteur (314) pour décompter le signal d'horloge système (ϕ_1) un nombre prédéterminé de fois afin de générer un signal de retenue pour appliquer le signal de retenue, en tant que signal de remise à zéro, à ladite bascule (312).

14. Un circuit selon la revendication 12 ou 13, dans lequel ladite unité de sélection d'adresse et de lecture/écriture (320) comprend :

- un inverseur pour inverser (221) le signal de fin dudit signal V-RLSA;
- un sélectionneur (322) qui répond audit signal de fin dudit circuit V-RLSA pour sélectionner le signal d'adresse horizontal dudit circuit H-RLSA ou la valeur de comptage fournie par ladite unité fournissant le signal d'horloge système et les adresses (310), le signal sélectionné étant émis en sortie en tant que signal d'adresse horizontal;
  un sélectionneur (322) qui répond audit signal de fin dudit circuit V-RLSA pour sélectionner le signal d'adresse vertical dudit circuit V-RLSA ou la valeur de comptage fournie par ladite unité fournissant le signal d'horloge système et les adresses (310), le signal sélectionné étant émis en sortie en tant que signal d'adresse vertical;
- un sélectionneur (324) qui répond audit signal de fin dudit circuit V-RLSA pour sélectionner l'un parmi, d'une part, les signaux de commande de lecture/écriture horizontale dudit circuit H-RLSA, et, d'autre part, le signal d'horloge système (ϕ_1), afin de fournir en sortie le signal sélectionné en tant que signal de commande de lecture/écriture horizontale; et
- un sélectionneur (325) qui répond audit signal de fin dudit circuit V-RLSA ainsi qu'à un signal de sortie dudit inverseur (221) afin de fournir le signal sélectionné en tant que signal de commande de lecture/écriture vertical.

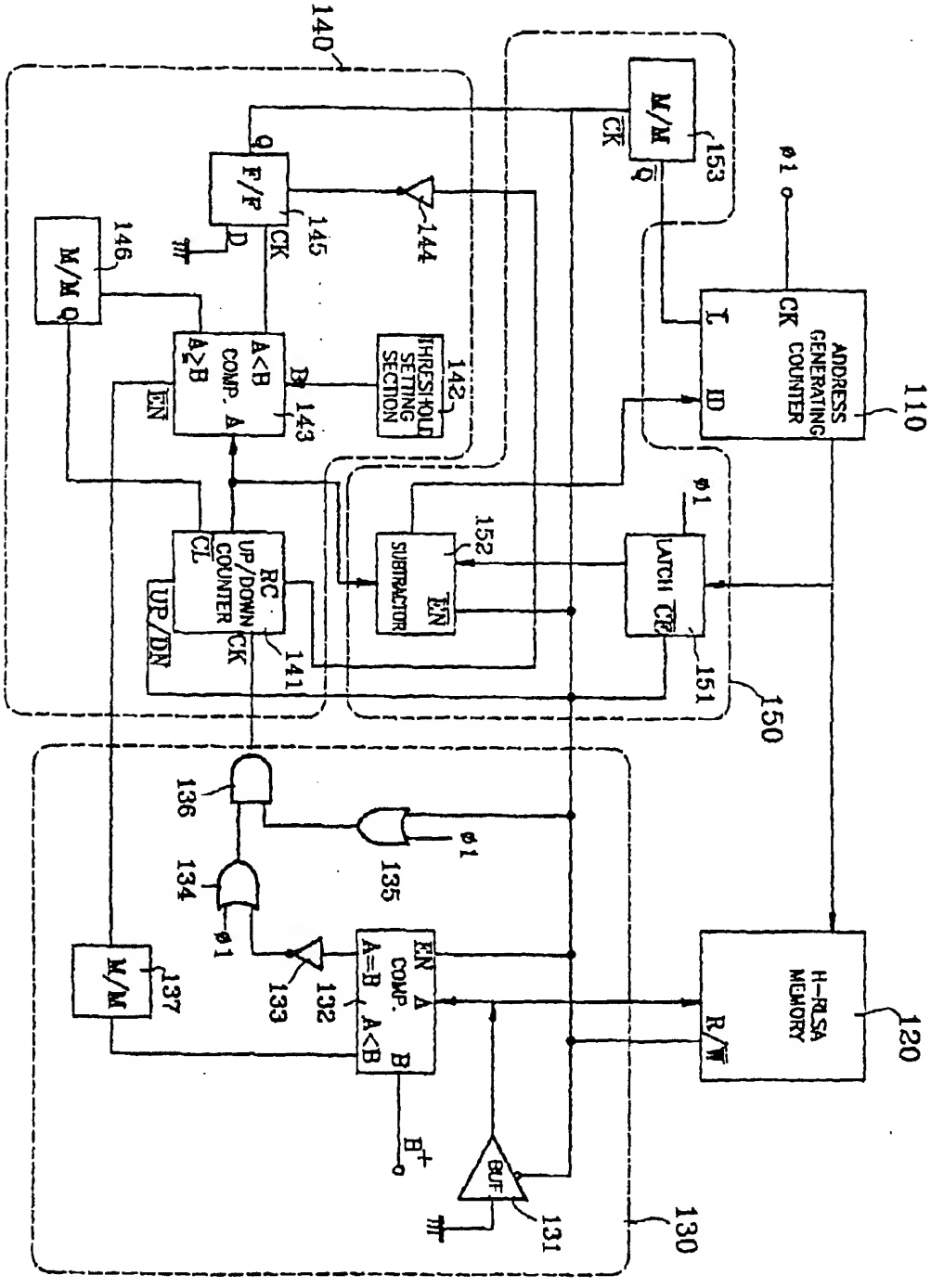
140
M/M
153
CK
Q
ø1
F/F
144
145
CK
D
146
M/M
A<B
A≥B
EN
B
143
142
THRESHOLD SETTING SECTION
ADDRESS GENERATING COUNTER
110
L
ID
ø1
152
SUBTRACTOR
EN
LATCH
151
150
RC UP/DOWN COUNTER
CL
UP/DN
CK
141
136
134
135
ø1
ø1
M/M
137
133
132
EN
A
COMP.
A=B
A<B
B
H+
BUF
131
130
H-RLSA MEMORY
R/W
120

FIG. 1

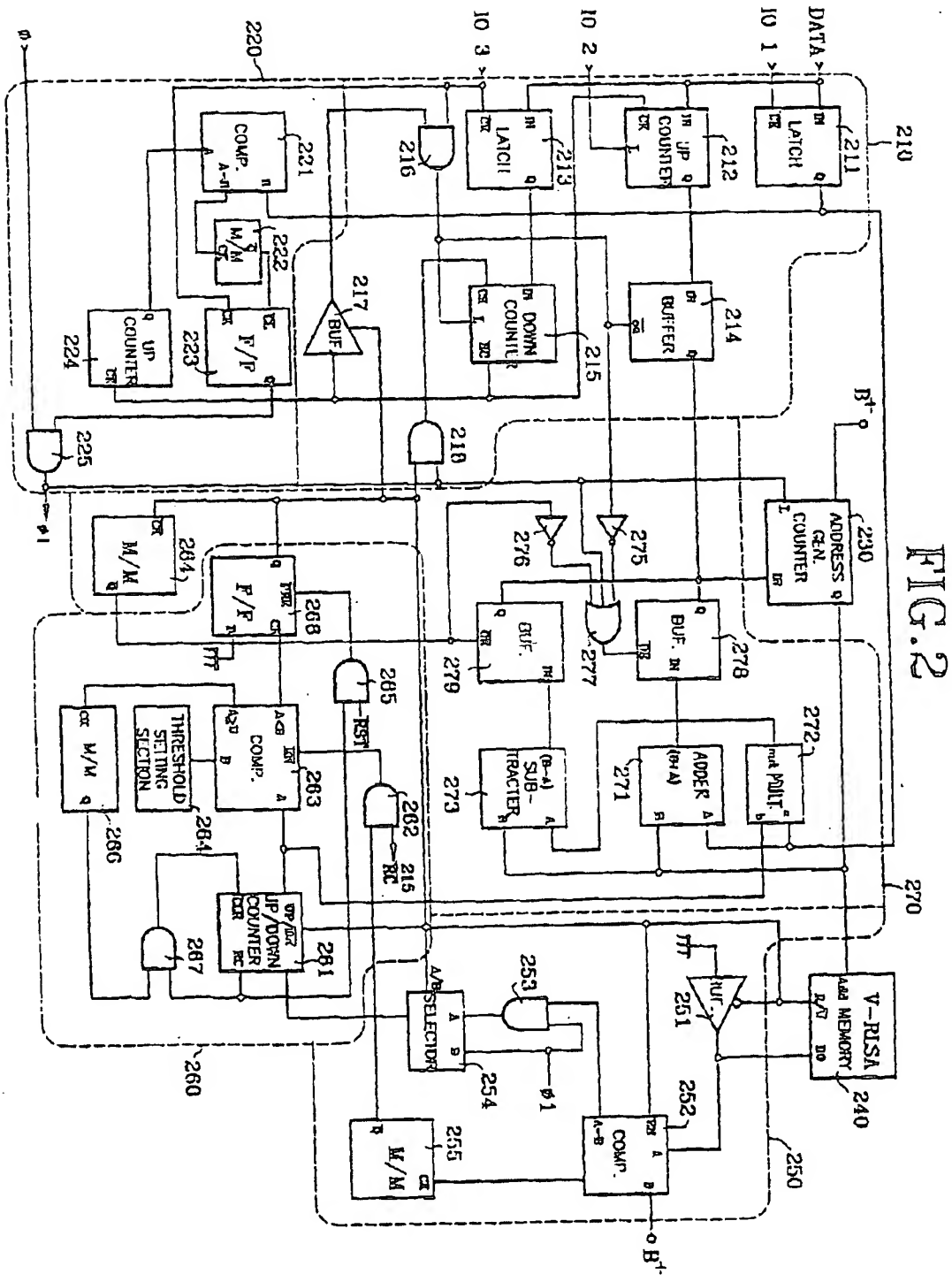
DATA
IO 1
IO 2
IO 3
Φ
Φ1
B+
LATCH
UP COUNTER
LATCH
DOWN COUNTER
BUFFER
COMP.
M/M
F/F
UP COUNTER
BUF.
ADDRESS GEN. COUNTER
BUF.
BUF.
ADDER
SUB-TRACTER
MULT.
V-RUSA MEMORY
THRESHOLD SETTING SELECTOR
COMP.
UP/DOWN COUNTER
SELECTOR
INV.
COMP.
M/M
M/M
RST
210
211
212
213
214
215
216
217
218
220
221
222
223
224
225
230
240
250
251
252
253
254
255
260
261
262
263
264
266
267
268
270
271
272
273
275
276
277
278
279
280

FIG.2

FIG.3A

	1	2	3	4	5	6	7	8
1	1	1	1	0	0	0	1	1
2	1	1	1	0	0	1	1	1
3	0	0	0	1	1	0	0	1
4	0	0	1	0	1	0	0	0
5	0	1	1	0	1	0	0	0
6	1	1	1	1	0	1	1	1
7	1	0	1	1	0	1	1	1
8	1	0	1	1	0	1	1	1
9	1	0	1	1	0	1	1	1

FIG.3B

0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	0
0	0	1	0	1	0	0	0
1	0	1	1	0	1	1	1
1	0	1	1	0	1	1	1
1	0	1	1	0	1	1	1
1	0	1	1	0	1	1	1

FIG.4

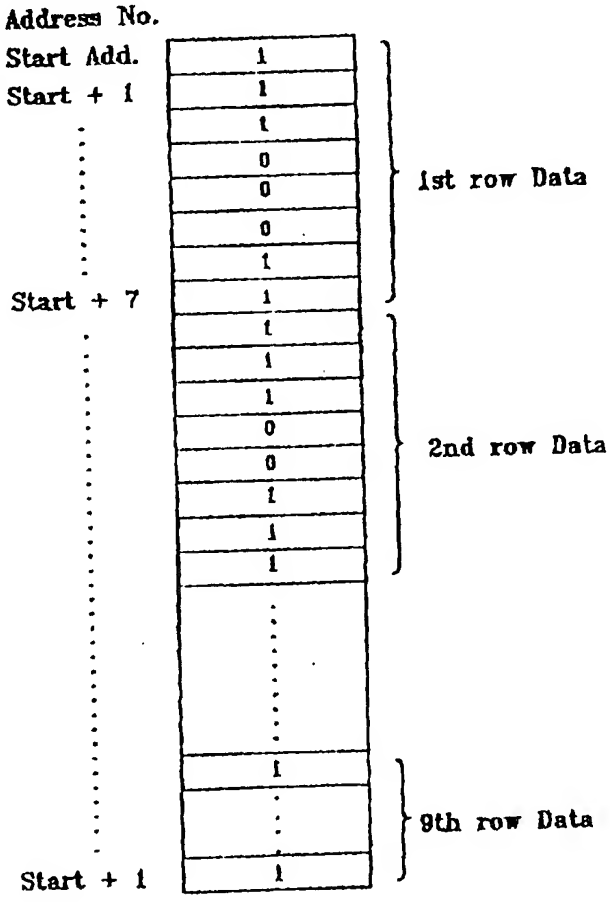

FIG.5

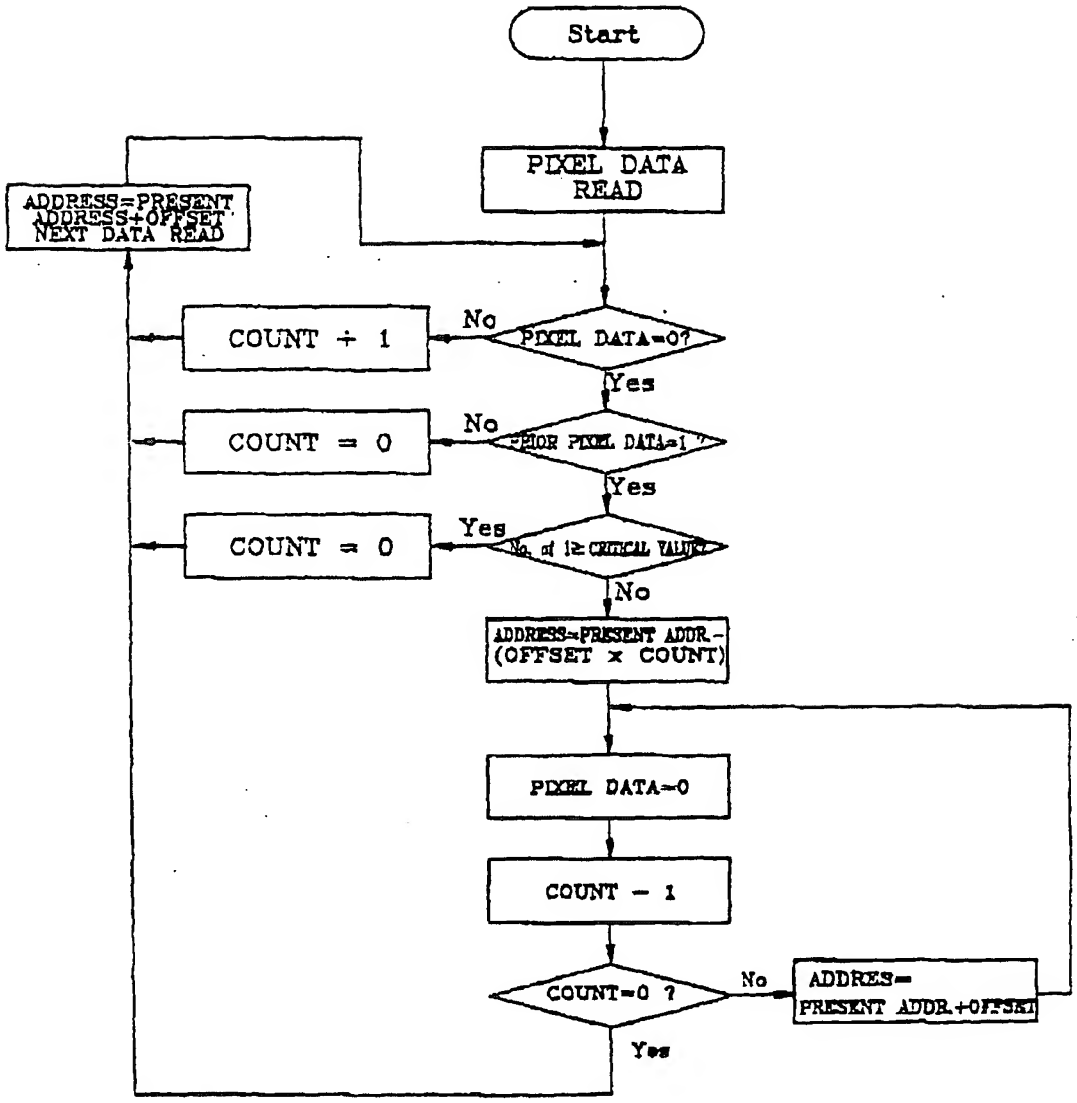
Start
PIXEL DATA READ
ADDRESS=PRESENT ADDRESS+OFFSET NEXT DATA READ
COUNT + 1
No
PIXEL DATA=0?
Yes
COUNT = 0
No
PRIOR PIXEL DATA=1 ?
Yes
COUNT = 0
Yes
No. of 1≥CRITICAL VALUE?
No
ADDRESS=PRESENT ADDR.-(OFFSET x COUNT)
PIXEL DATA=0
COUNT - 1
COUNT=0 ?
No
ADDRES= PRESENT ADDR.+OFFSET
Yes

FIG.6

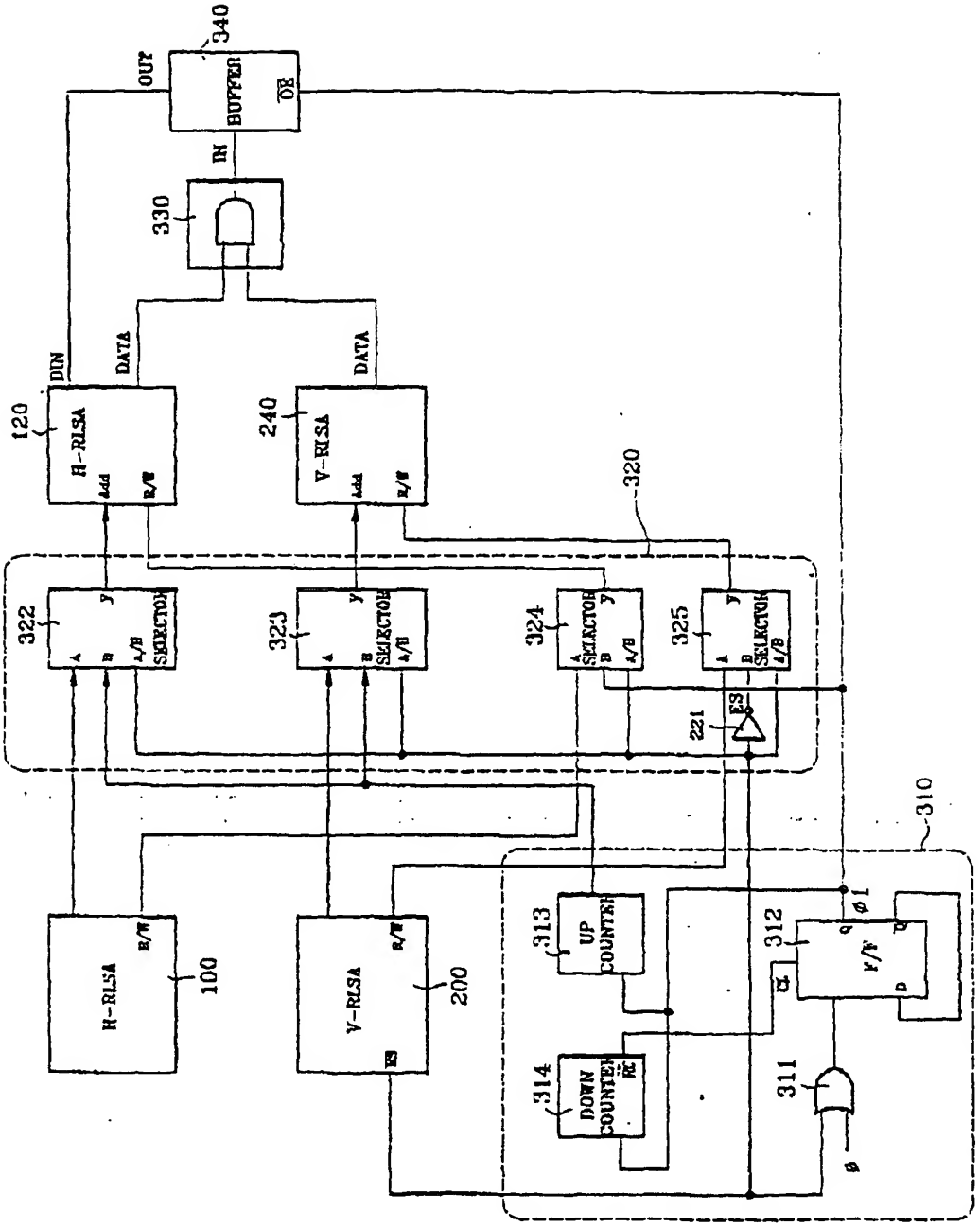
340
OUT
BUFFER
OE
IN
330
DIN
DATA
DATA
120
H-RLSA
240
V-RLSA
320
322
323
324
325
SELECTOR
221
310
313
UP COUNTER
312
314
DOWN COUNTER
311
H-RLSA
100
V-RLSA
200

FIG.7A

FIG.7B

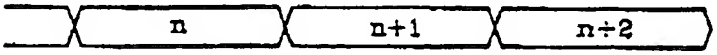

FIG.7C

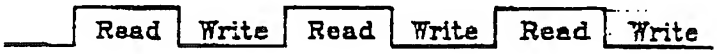

FIG.7D

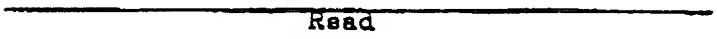

FIG.7E

FIG.7F

FIG.8A

1	1	1	0	0
1	1	1	1	0
0	0	0	1	1
0	0	0	1	1
0	0	0	1	1

FIG.8B

1	1	1	0	0
1	1	1	0	0
1	1	1	1	1
1	1	1	1	1
1	1	1	1	1

FIG.8C

1	1	1	0	0
1	1	1	0	0
0	0	0	1	1
0	0	0	1	1
0	0	0	1	1